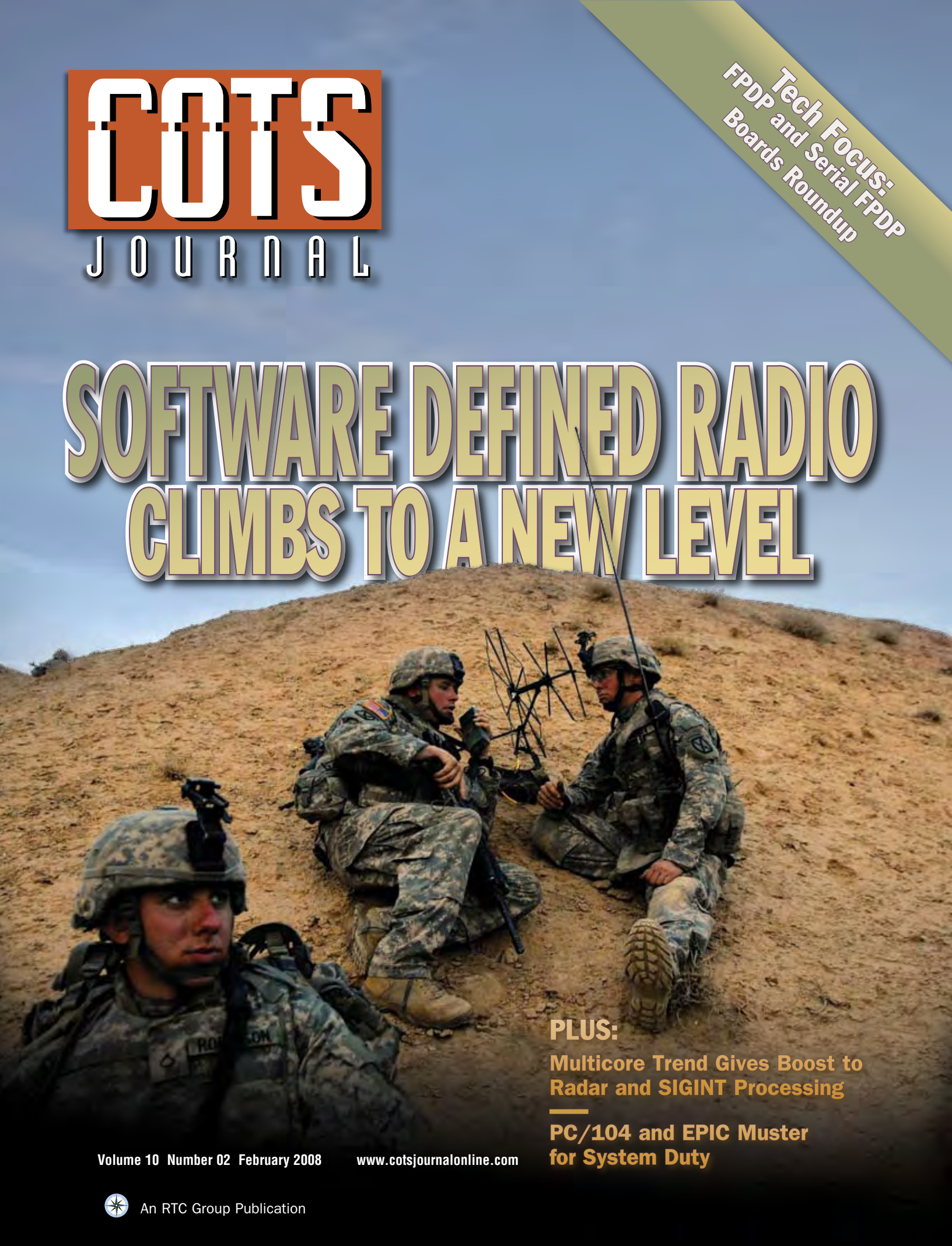
COTS JOURNAL

Tech Focus: FPDP and Serial FPDP Boards Roundup

SOFTWARE DEFINED RADIO CLIMBS TO A NEW LEVEL



PLUS:

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COTS JOURNAL

Features

February 2008 Volume 10 Number 2

Special Feature

Software Defined Radio

Tech Recon

Multicore in Radar and SIGINT

System Development

PC/104 and EPIC

Technology Focus

FPDP and Serial FPDP Boards

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Departments

Coming in March...
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Now in development, Joint Tactical Radio System (JTRS) radios require a software defined architecture that supports multiple protocols while providing standardized hardware that can implement a broad range of systems from simple baseband to complex wideband radios. Shown here, U.S. Army soldiers from Charlie Company, 2nd Battalion, 22nd Infantry Regiment, 1st Brigade Combat Team, 10th Mountain Division, make radio contact with 1st Brigade during a three-day air assault mission along the Zaghytun Chay River in Iraq.

Courtesy: U.S. Air Force photo by Staff Sgt. Samuel Bendet

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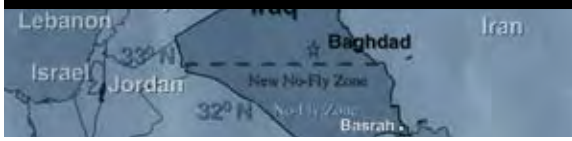


Andy Rooney Wannabe

This is going to be another one of those columns where I get lots of e-mails complaining that I shouldn't be complaining. I'm waiting for the day that computers—without any human intervention or judgment—start producing the news. It may just be my age and that I'm starting to think too much like Andy Rooney from 60 Minutes. Yes, I know it's wrong to "every" when you haven't experienced "every," but it seems every commercial news outlet—especially electronic ones—are producing shows to obtain market share. The shows are dependent on obtaining and maintaining a sufficiently large enough audience in order to sell advertising that pays for management and produces a profit for the stockholders. The way news organizations maintain their audience is by selecting issues to talk about and, let me call it "selecting a slant" in the presentation that appeals to their particular target audience. In other words, through means that would make Edward R. Murrow turn in his grave.

One day late last year all the news media local to where I live ran teaser sound bites all day about contamination at a local water treatment plant. Then at 11:00 PM they had these big stories about organic contamination at the water treatment plant. Not once did they say it was a wastewater treatment plant. I'm not sure how you contaminate a wastewater treatment plant with organics. Isn't that what they're treating in the first place? But I'm sure most of the audience thought that the story would be about drinking water. Along the same lines, just listen to all the different television media reports on the same Presidential candidate's speech—you'd think each was about a different speech or person. All that has relegated me to watch *BBC World News* in order to be able to get some frame of reality on what's going on in my own country. And—again before you e-mail me—print news media isn't any different.

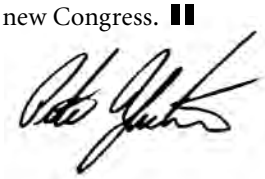
I guess the cherry on this cake is e-mail. Every one of my relatives, friends and a lot of strangers seem to have a need to e-mail me jokes and commentary that support their political views or candidates. Now I have to be honest: 99% of the stuff I get is in line with what they think my political views are. So, why do they send these things? Is it that they think I may sway from my opinion? Or that this junk will further bolster my opinion? Or that I might forward it to someone who needs swaying?

Studies have shown that the Web and the Internet have had a profound and increasing effect on obtaining support for political views or candidates. I don't go on blogs of any kind, nor do I listen to radio talk shows. I don't really care about most people's opinions. Again, you're going to feel the urge to e-mail me on this. Please don't. My view of people who call in on radio talk shows, or get on to blogs is that they're either looking to sell or promote something, trying to attain their moment of fame, trying to find someone that will communicate with them, or…and so and so. If there is a subject that I want to explore, I know the people to contact that will have valid information and I contact them. I don't throw up a jump ball for anyone on earth to respond to.

I know I'm going to get a lot of heat for everything I said here, including internally. Most publications—including some of the RTC Group's—have blogs, so not sounding overly enthusiastic about this medium may not be the most intelligent thing to do. But then again I did say I may be getting to be a little too much like Andy Rooney. Also, if I weren't dead honest I'd be like the news media I'm complaining about. Our marketplace has a lot of good publications—of which I think *COTS Journal* is one—and when I read an article by an editor that's covering our market, I don't go on a blog to respond, I e-mail them directly. In most cases it's to let them know that I think they did a great job in covering a subject. There have been a few instances where I suggested some considerations they may wish to explore when covering a subject. And I do that more to ensure that they produce a better story the next time rather than to complain.

Our marketplace tends to have a large number of publications that actually do try to provide useful and insightful information. And when they do that they end up with focused and quality readership. Believe it or not having quality readers stimulates quality, timely, focused editorial. Editors have interplay with their readers—they are their sounding board with what needs to be explored. Now, will blogs enhance that interplay or just provide a diversion? I think you know my view.

Well I don't think that my rant here comes close to anything Andy Rooney would have done, so I don't think I'll do this again—at least for a while. Enjoy the political news and promotion season. Our pain should end in about nine months. But then we'll need to hear all the speculation on the President elect and the new Congress. ▮▮



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The Inside Track

Lockheed Taps Sandia's Java Rule Engine for Navy's DDG 1000 Ship

Lockheed Martin has licensed Jess 7.1a3, a popular rule engine created by Sandia National Laboratories, to play a critical role in the Navy's DDG 1000 destroyer ships. The company reportedly chose Jess after extensive and multiple trade studies confirmed the software's ability to interface with the information in the DDG 1000 knowledgebase. Jess was licensed by Lockheed Martin Simulation, Training & Support (STS), a business unit within the company's Electronics Systems business area. STS is a leader in the development of logistics solutions and military training and simulation, producing air, ground and maritime systems for customers worldwide.

Figure 1

Shown here in this concept image, the Navy's DDG 1000 is a multi-mission, maritime fleet of destroyer ships. The ships feature an integrated power system, dual-band radar, integrated undersea warfare system and advanced gun system.

The Navy's DDG 1000 (Figure 1) is a multi-mission, maritime fleet of destroyer ships. It includes a number of advanced technologies and features, including an integrated power system, dual-band radar, integrated undersea warfare system and advanced gun system. Among other intended uses, Jess will help the DDG 1000 ship domain controller with its alarm management function and reasoning about ship system states for safe operation. Jess enables software developers to embed intelligence in the form of business rules directly into their Java applications. Jess is an integrated development environment (IDE) for rules that increases programmer productivity and enhances collaboration. The IDE is based on the Eclipse platform and features tools for creating, editing, visualizing, monitoring and debugging rules.

Sandia National Laboratories
Livermore, CA.
(925) 294-3358.
[www.sandia.gov].

Harris to Provide Comms System for American Forces Network

Harris has been awarded a contract from broadcast systems integrator Snader and Associates to provide a comprehensive broadcast communications system for the American Forces Network. The American Forces Network delivers news, information and entertainment to almost one million troops worldwide outside of the United States.

Snader and Associates is designing the new broadcast system, which will be installed at the Defense Media Center in Riverside, California, and is expected to be completed in the summer of 2008. Under the agreement, Harris will provide broadcast routing, automation, video servers, core processing and asset management products. The system includes the first members of the new Harris NEXIO AMP product family—the NX3601HDI media platform with integrated storage and the NX3601HDX media platform for use on a NEXIO storage area network. NEXIO AMP pairs a high-performance, high-definition/standard-definition (HD/SD) server architecture with best-in-class content protection. The new system combines the highest levels of I/O, data pathway and storage redundancy with all the features broadcasters have come to expect in NEXIO\ servers— including integrated software codec support and automatic up/down/cross conversion.

Harris
Melbourne, FL.
(321) 727-9100.
[www.harris.com].

L-3 to Integrate its Imagery Suite into Marine Corp Workstations

The U.S. Navy has awarded L-3 Communications a contract to acquire and integrate its VideoScout video exploitation and management components into the Marine Corps' Tactical Exploitation Group's (TEG) Remote Workstation System. The TEG is the primary tactical imagery exploitation system in the Marine Corps, supporting the highly mobile Marine Expeditionary Force (MEF).

VideoScout (Figure 2) will provide imagery analysts with a more effective means to exploit, map, archive, search, retrieve

Figure 2

VideoScout provides imagery analysts with a more effective means to exploit, map, archive, search, retrieve and disseminate critical video and telemetry data received from a variety sources like UAVs, sensors and INTEL networks.

and disseminate critical video and telemetry data received from a variety of manned and unmanned aerial vehicles (UAVs), sensors and INTEL networks. This helps improve mission planning, mission execution, targeting, battle damage assessment and post-mission analysis. By integrating VideoScout into mobile workstations, field personnel can quickly exploit, manage and disseminate imagery, video and metadata from any source, providing real-time shared situational awareness across the battle space. The Navy has issued its first purchase order for VideoScout Flex, which includes both video/image processing hardware and video exploitation/management software components designed for easy integration into existing computer systems.

L-3 Communications
San Diego, CA.
(858) 552-9600.
[www.L-3Com.com].

Parvus Rugged Ethernet Switch Node Drafted for Apache Upgrade Program

The Aviation Applied Technology Directorate has specified the DuraNET 1059 Ethernet switch node from Parvus into a U.S. Army aviation modernization program for the AH-64 Apache helicopter (Figure 3). Orders for 34 units have been received by Parvus to-date. Part of the U.S. Army Research, Development & Engineering Command (RDECOM), AATD is a Directorate of the Aviation and Missile Research Development and Engineering Center (AMRDEC) located at FT. Eustis, Virginia. AATD's mission is to be recognized as the leader within the Department of Defense (DoD) for the research, development and engineering of rotorcraft and tactical unmanned aerial vehicle (UAV) systems and technology.

Figure 3

The modernization program for the AH-64 Apache helicopter is aimed at improving situational awareness. The Ethernet switch node will provide a link to onboard IP-enabled computing devices.

Parvus' DuraNET 1059 will be installed on several AH-64 Apache helicopters in early 2008 under a U.S. Army Quick Reaction Capability (QRC) initiative aimed at improving situational awareness. This rugged, unmanaged Ethernet switch node will provide local area network (LAN) connectivity to onboard IP-enabled computing devices. Weighing in at less than 2 lbs and equipped with MIL-38999 connectors, a conductively cooled chassis and MIL-STD-704E-compliant power supply, the rugged Fast Ethernet switch module is suited for airborne or ground vehicle networking applications.

Parvus
Salt Lake City, UT.
(801) 483-1533.
[www.parvus.com].

Team Completes Test and Design Review for Army's WIN-T Increment

General Dynamics C4 Systems and teammate Lockheed Martin have successfully completed the engineering field test and preliminary design review for Increment Two of the Warfighter Information Network-Tactical (WIN-T), which means the program is on schedule to conduct limited user tests in 2008 and deploy new technology to soldiers in 2009. WIN-T Increment Two provides a mobile broadband network that will enable commanders and command posts to carry out battle plans and to collaborate while on-the-move.

The engineering field test conducted at Ft. Dix and Lakehurst Naval Station in New Jersey, provided a means to assess technical maturity of key features needed for network mobility. These technology features include the Network Centric Waveform, which enables mobile platforms to access the WIN-T network; the Highband Networking Waveform, a wideband, wireless wide area networking capability; and the WIN-T Network Management System, which uses commercial-standard network and systems management protocols and interfaces to provide the necessary automation to keep mobile forces networked. The preliminary design review, a detailed analysis of the system design to determine that it meets the documented performance and engineering requirements, was conducted in Foxboro, Mass.

General Dynamics C4 Systems
Scottsdale, AZ.
(480) 441-3033.
[www.gdc4s.com].

Performance Tech Boards Chosen for Navy E-6B Aircraft Upgrade

Performance Technologies announced that it is working with Rockwell Collins in delivering an upgrade to the Navy's E-6B Mercury aircraft. The Mercury (Figure 4), a communications relay and strategic airborne command post aircraft, provides survivable, reliable and endurable airborne command, control and communications between the National Command Authority (NCA) and U.S. strategic and non-strategic forces.

As part of the aircraft's internal electronics upgrade through Rockwell Collins, Performance Technologies' embedded CompactPCI hardware components will be integrated on board the aircraft for improved communication, control/monitor functions and networking. Components include the company's Intelligent Shelf Manager (ISM) that provides remote systems monitoring and diagnostics, Ethernet switches and chassis mid-planes.

Performance Technologies
Rochester, NY.
(585) 256-0200.
[www.pt.com].

Figure 4

The Navy's E-6B Mercury is a communications relay and strategic airborne command post aircraft, which provides survivable, reliable and endurable airborne command, control and communications between the National Command Authority (NCA) and U.S. strategic and non-strategic forces.

COTS Websites

www.dtic.mil

Search Engine Is a "Gateway" to Info on Military Technology

The Defense Technical Information Center (DTIC) was fielded with a daunting mission in mind: to sort and organize the DoD's array of technology-related activities, laboratories and information resources. Its Web site is the centerpiece of that mission. The DTIC provides centralized operation of DoD services for the acquisition, storage, retrieval and dissemination of Scientific and Technical Information (STI) to support DoD research, development, engineering and studies programs. And now it offers a feature called DTIC Search. It lets visitors search for science and technology information across all DoD sectors and beyond. This includes many defense agencies, unified commands, the military services—Army, Navy, Air Force, Marine Corps—and other elements of the defense

and military establishments. It can also be configured to coordinate searches with your favorite search engine, such as Google or FirstGov, or even search only on ".mil" Web sites using those engines.

DTIC also hosts a variety of databases. Its Technical Report Database contains nearly two million reports in print and electronic form conveying the results of Defense-sponsored research, development, test and evaluation (RDT&E) efforts. DTIC has also acquired Library of Congress Federal Research Division records that cover a variety of foreign and domestic subject areas. A Research Summaries Database contains descriptions of DoD research that provide information on technical content, responsible individuals and organizations, principal investigators and funding sources at the work-unit level. And finally, DTIC's Independent Research and Development (IR&D) Database has over 165,000 descriptions of R&D projects initiated by DoD contractors but not performed under contract.

Defense Technical Information Center
Fort Belvoir, VA.
1-800-225-3842.
[www.dtic.mil].

Special Feature

Software Defined Radio

SDR: Is the Technology Catching Up to the Vision?

The theme of the SDR Forum's 2008 Technical Conference is "SDR 2.0—Entering the Mainstream." And maybe that's just what's finally happening.

David B. Cotton
Contributing Editor

For quite a number of years, the vision of reconfigurable or software defined radios appeared to be just that—a vision. But now it seems that the technology is catching up with the vision. At least, that's the opinion of Lee Pucker, the new CEO of the Software Defined Radio Forum.

Software defined radio (SDR) is rapidly becoming a very broad field, and to understand fully what's happening in the field, one needs to look at three different areas. The first one is the U.S. military's Joint Tactical Radio System (JTRS) program and its contractors and subcontractors; the second is suppliers of hardware and software components to both worldwide military contractors and the general market; and the third is the SDR Forum, which attempts, on an international scale, to bring together all interested parties, to push for standards and to promote progress in all areas related to software radio.

The JTRS Picture

Although the JTRS program has been around for quite a while, several years ago it was totally reorganized under the Joint Program Executive Office (JPOE) and its then-existing five Clusters of programs were recast into four Domains, some of which contained multiple programs (Table 1). And, in the past year, some progress has been apparent.

The JTRS Domains		Status
Ground Domain	• Ground Mobile Radio (GMR) (formerly Cluster 1): Support requirements for Army & Marine Corps Ground Vehicular platforms. • Handheld/Manpack/Small Form Factor (HMS) (formerly Cluster 5): Support requirements for JTRS handheld & manpack units and forms suitable for integration into platforms requiring a Small Form Fit radio.	• GMR: contract awarded to team headed by Boeing. Initial production begun on Engineering Design Models (EDMs) with formal certification and field testing to begin in late 2008. Earlier pre-EDM versions have been under test for some time. • HMS: contract awarded to team headed by General Dynamics C4 Systems (GDC4S). Pre-engineering development models & 2-Channel Manpack Technology Demonstrators delivered for evaluation.
Airborne, Marine and Fixed Domain	• Airborne, Marine and Fixed Site (AMF): Support requirements for airborne (including rotary wing), marine and fixed station platforms for all Services. • Multifunctional Information Distribution System—JTRS (MIDS-J): Migrate the current MIDS—Low Volume Terminal to MIDS—JTRS compliance producing the next generation data link and communication terminal for joint and coalition tactical platforms.	• Expectation is that the AMF contract will be awarded at the end of February 2008 (delayed from last quarter of 2007). Boeing and Lockheed Martin lead teams bidding on this contract. • MIDS-J team led by Data Link Solutions (DLS), a joint venture of BAE Systems—Rockwell Collins. High performance, open-architecture, Link 16 terminals for fighter aircraft, ships and command and control centers.
Network Enterprise Domain	Waveform Program Office: Responsible for waveform development, cryptographic equipment applications, architectural integrity of JTRS, gateways and common network services.	JTRS Bowman Waveform certified as compliant with JTRS Software Communication Architecture (SCA), allowing it to be integrated into JTRS radio products. Bowman Waveform allows tactical command and control interoperability between UK and US forces.
Special Radio Systems	JEM = JTRS Enhanced Multi-Band, Inter/Intra Team Radio (MBITR) (formerly Cluster 2): Managed by Special Operations Command: Support requirements for handheld radios for the Army, Navy, Marine Corps and Air Force Special Operations Forces.	Thales Communications named prime contractor, to evolve battle-proven MBITR into JEM.

Table 1

JTRS Program Domains and their status.

Within the Ground Domain, Boeing, the prime contractor for the JTRS Ground Mobile Radio (GMR) program, announced in January 2008 that it had begun production of GMR Engineering Design Models (EDMs), which will undergo field and system regression testing during this year. Earlier—in March 2007—General Dynamics C4 Systems (GDC4S), the prime contractor for the JTRS Handheld, Manpack and Small Form Fit (HMS) program, delivered pre-engineering development models and 2-Channel Manpack Technology Demonstrators for evaluation (Figure 1), which are also undergoing evaluation and testing.

In the Airborne, Marine and Fixed (AMF) Domain, in late 2007 it was announced that the AMF contract award had been delayed until early 2008, probably February. Boeing and Lockheed Martin lead multiple-company teams bidding on this contract. Also within this Domain, the Multifunctional Information Distribution System-JTRS (MIDS-J) program is working to provide a next-generation data link and communication terminal for joint military and coalition tactical platforms. This program is managed by Data Link Solutions (DLS), a joint venture of BAE Systems and Rockwell Collins.

The Network Domain contains the Waveform Program Office, which is responsible for waveform development in addition to cryptographic applications, gateways and common network services and the architectural integrity of JTRS. In November 2007, the JPOE announced certification of the JTRS Bowman Waveform as compliant with the JTRS Software Communication Architecture (SCA), thus allowing it to be used in communications between UK and U.S. forces. And, in the Special Radio Systems Domain, Thales Communications was named as the prime contractor to evolve the battle-proven Multi-Band Inner/Intra Team Radio (MBITR) into its JTRS-compliant successor, the JTRS Enhanced Multi-Band Inner/Intra Team Radio (JEM).

Figure 1

General Dynamics C4 Systems' JTRS Manpack prototype for the Handheld, Manpack and Small Form Fit (HMS) program.

Figure 2

Pentek Model 7140-420 Dual Digital Transceiver with Wideband Digital Downconverter (DDC).

On the Commercial Front

In addition to the JTRS military contractors and their subcontractors, there are a number of firms engaged in supplying hardware and/or software in support of the software radio field. A significant number of these are based outside the U.S.—in Canada or the UK—and relationships or joint ventures are being undertaken with other companies in Europe or Asia. Let's look at some of the key developments in the past year.

GE Fanuc purchased Radstone and their ICS division. Late in 2007, they announced the ICS-8551 rugged ADC PMC/XMC module as a digital receiver for SDR applications such as spectrum monitoring, signal intelligence and tactical communications. The ICS-8560 PMC/XMC digital transmitter module followed shortly thereafter.

Hypres is a leading developer of superconductor microelectronics (SME) technology and the supplier of the Digital RF product line. In 2007, it partnered with SELEX Communications, an Italian company, to develop an all-digital receiver to be used with the software radio under development by SELEX.

In June 2007, Lyrtech, one of the Canadian companies in SDR, launched its OBSAI/CPRI Virtex-4 Development Platform using the new Xilinx OBSAI RP3/RP3-01 and CPRI reference designs developed by Xilinx as part of the 3G Wireless Base Station Initiative. This was followed, in November 2007, by the release of its SCA implementation on the Small Form Factor SDR Development Platform (SFF SDR DP). The latter integrates the SCARI Software Suite from Communications Research Centre Canada (CRC), an object request broker (ORB*express*) from Object Interface Systems (OIS) and software from Green Hills with other technologies from Lyrtech.

In July 2007, Pentek expanded its VME product line by releasing its Model 7140-420 Dual Digital Transceiver with Wideband Digital Downconverter (DDC) Core and Interpolation Filter—a complete software radio in a PMC/XMC module (Figure 2). It is also available in PCI, 3U and 6U cPCI and conduction-cooled PMC/XMC versions.

PrismTech, a vendor of high-performance SDR middleware and tooling, had a busy year. First, they put their Spectra Operating Environment (OE) on the Gumstix family of small form-factor computers—so named because they are open source Linux miniature computers about the size of a stick of gum. Next, PrismTech introduced their second-generation Spectra 2 OE. They also completed a study for the JPOE to help define waveform portability guidelines for the JTRS program. And they worked with Rockwell Collins to bundle the latter's FlexNet Four Radio with PrismTech's Spectra SDR development products.

In May 2007, Vecima Networks, also of Canada, purchased Spectrum Signal Processing, another Canadian SDR company. In August 2007, Spectrum, now known as Spectrum Signal Processing by

Vecima, introduced a new member of its flexComm family—a Public Safety Cross Band Communications Platform—an integrated wireless communications subsystem designed to speed up the time to deployment of first responder communications services (Figure 3). Then, in September, Spectrum announced support for the JTRS Modem Hardware Abstraction Layer (MHAL) application programming interfaces (APIs). In October, they made public their intent to offer physical layer implementations of military communications (MILCOM) and satellite communications (SATCOM) waveforms, including ones key to JTRS and NATO. In addition, they also announced the rugged flexComm 4800, a family of embedded radio modules for MILCOM and SATCOM applications.

Zeligsoft—still another Canadian company involved in software radio—integrated its SDR development tool, Zeligsoft Component Enabler (Zeligsoft CE), with the Software Defined Radio Core Framework (SDR CF) of Electrobit Corporation (EB) of Finland. EB's SDR CF is reputed to be the first European-developed, SCA-compliant CF implementation. In addition, Zeligsoft reported that its CE and Code Generator now support an end-to-end design flow with The MathWorks' Simulink and Real-Time Workshop products.

What's New with the SDR Forum?

The SDR Forum provides a medium for the exchange of ideas between key players and companies in the software radio field. One way is through periodic reports on key subjects of broad interest.

This past year, the SDR Forum released an 84-page report—"The U.S. Public Safety Market"—which points out the communications problems within and across the multiple organizations, including federal, state and local; city, county and regional; police, fire and medical emergency that make up this market. One of its findings was that without consistent and adequate policies, standards and guidelines regarding public safety communications systems, first responders not only have problems communicating effectively during stressful emergency situations, but they can often lack the means to coordinate their most routine activities. Of course, the SDR Forum sees software radio playing a role in solving these problems.

During the year, the Forum also released a 62-page study entitled "The Cognitive Radio Market." A cognitive radio (CR) is one that intelligently determines which communication channels are currently in use and automatically switches to an unoccupied channel. This technology has inspired a vision of "multimedia wireless services anywhere, anytime and with any device." Since, in the future, the key wireless industry segments include commercial, public safety and military, there is much interest in CR as an enabling technology and software radio as a means of providing it.

In addition to its studies, the SDR Forum holds multiple general meetings per year—held in various regions around the

Figure 3

Public Safety Cross Band Communications Platform from Spectrum Signal Processing by Vecima.

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globe—and an annual technical conference and exposition. All of these are used to provide tutorials, present papers and, in the case of the exposition, showcase current developments in order to spread the software radio message and recruit and involve more participants. The theme of their 2008 Technical Conference, to be held in late October, is "SDR 2.0 – Entering the Mainstream." And maybe that's just what's finally happening. ▮▮

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The Myths and Realities of Code Portability

Code portability problems arise because the developer and a reuser may be in competitive organizations. Because the developer pays the burdens of designing for reuse while the benefits accrue to the reuser, in order to ensure success a business model is necessary to incent the developer to bear this cost.

Manuel Uhm, Senior Marketing Manager and
Chad Epifanio, Waveform Product Manager,
Processing Solutions Group, Xilinx, Inc.

Code portability, or code reuse, is a long-standing technique to reduce system development costs. It forms a key tenet of the Joint Tactical Radio System (JTRS) and other transformational defense programs. However, a number of preconditions must be met in order to reap significant cost reductions. Improper reuse may actually have the undesired effect of increasing development costs. Furthermore, there may be better methods for reducing system cost, as coding is, in fact, not the most costly aspect of development.

Let's explore the myths and realities of code portability with a particular emphasis on identifying those preconditions and contrasting them against some of the realities occurring in the field today. The focus will be on FPGA code, as both the difficulty and the need for portability are arguably greater than for GPP code, though the general concepts presented are applicable to all processors.

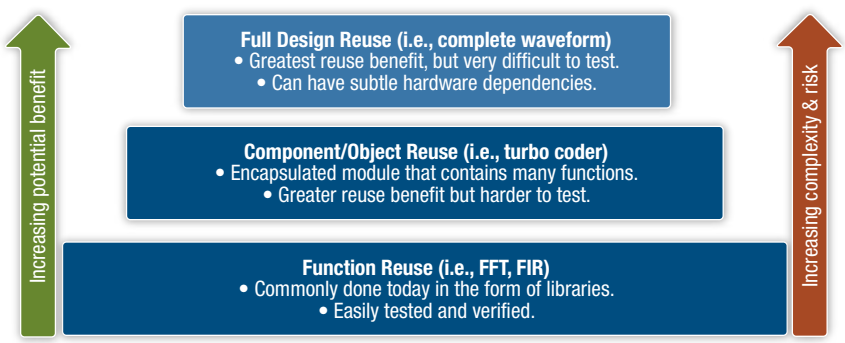

Figure 1

The range of code reuse and the trade-off between benefit and risk.

Many problems derive from the fact that the developer and the reuser may reside in different, sometimes competitive organizations. While the burdens of designing for reuse are borne by the developer, the benefits accrue to the reuser. To reliably succeed, a business model is necessary to incent the developer to bear this cost.

What is Code Portability?

To frame the discussion, we must first define what is meant by "portable code." In its most general sense, portable code is code that can be reused in another project. There are multiple levels of code reuse, as illustrated in Figure 1. At a basic level there is function reuse. This is fairly easy to achieve, as functions are small, coherent units that are easily tested and verified. We consider low-level IP cores, such as fast Fourier transforms (FFTs) or finite impulse response filters (FIRs), to be equivalent to a software function in terms of reuse. Component or object reuse provides greater benefit than function reuse, in that they are aggregations of functions and perform more complex tasks. They are also more difficult to test and verify under all expected operating conditions, but porting problems can still be localized fairly accurately.

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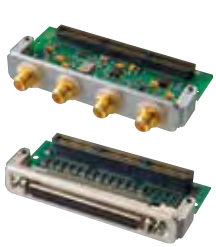

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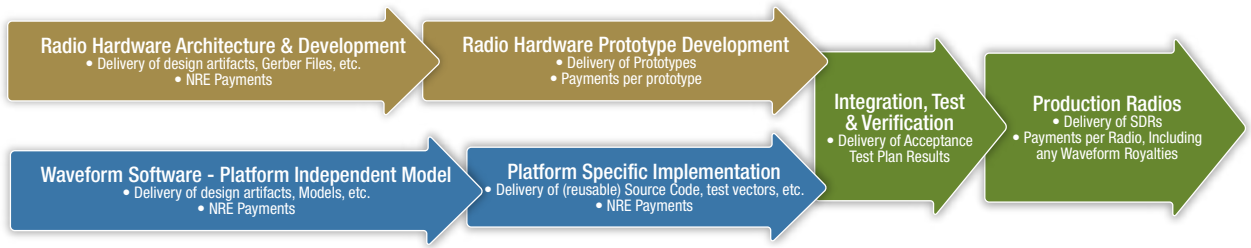

Figure 2

Potential SDR Business Model by Stage, Deliverables and Payment Model. *(Note: Simplified—not meant to be an all-inclusive list.)*

FPGA IP such as Forward Error Correction cores can be classified in this category. At the highest level, full design reuse, such as a complete waveform, provides potentially the greatest benefit, but is also the most difficult to attain. One reason is that it is difficult to test and verify the design over all anticipated operating conditions and deployment platforms. Porting problems can be very difficult to diagnose and repair, as they may be the result of subtle interactions between components that did not appear in the original host platform.

Some defense programs attempt to go even further by trying to leverage full design reuse across separate companies. This is a very difficult task. Again, the problem is that the burden is distributed unequally—the extra cost is borne by the developer, while the benefits accrue to the reuser. Furthermore, most companies consider the designs and code to be a source of competitive advantage, and so they are loath to provide it to the broader industry. On the other hand, code reuse within a company makes sense, since the company will benefit in the future from the extra effort incurred, while maintaining its competitive advantage. Developer altruism cannot be the basis of successful reuse. In these circumstances, there must be some carrot, in the form of a profit-driven business model, or some stick, in the form of enforceable portability standards and requirements.

Myth #1: Written Code Is Reusable Code

Reusable code is certainly possible, but does not come for free. The reuser must have confidence that the code to be reused not only behaves as advertised, but

will behave the same on the reuser's chosen platform. The way to build this confidence is to provide the reuser with all of the artifacts that went into the development of the code. These include:

- use cases or CONOPS (i.e., concept of operations),
- high- and low-level specifications,
- relevant trade studies,
- reference models, also known as base waveforms or platform independent models,
- fixed-point simulations, and
- test vectors.

The reuser must be able to verify that the requirements and use cases are either sufficiently similar so that the design can function in both use cases, or identify areas where they are not and modify the design accordingly. Good documentation is vital to successful reuse. The level of granularity is important; each coherent functional unit in the design should have documentation and test vectors. The test vectors must completely cover the operating space. Most systems can work great when there is no noise, multipath, or interference. The real test of a radio is behavior in extreme environmental conditions.

When trying to port large designs between disparate platforms, the reuser is almost assured to encounter anomalous behavior. Without functional unit descriptions and test vectors, the reuser has no choice but to start a tedious, and expensive, reverse engineering effort. The reuser must first identify what the code currently does, then try to infer what it was intended to do. From there, the reuser must forward-engineer a solution. This is where blind reuse without good documentation can actually end up being more expensive than designing it from scratch from base principles.

Myth #2: Executable Code Defines the Waveform

It should be noted that the final deployed executable code cannot be used as a means of specifying system behavior. The executable code is a specific implementation of a waveform, not the definition of it. Hence, it always has some amount of platform-specific detail. For example, it may contain software-hardware partitioning between a GPP and an FPGA, which may not be supportable by the reuser's platform. The ultimate definition of the waveform must be the top-level specifications.

Unfortunately, many military waveforms have specifications that are inadequate such that two independent waveform developers cannot build two independent systems and have any hope of them actually intercommunicating. Hence, it is necessary to have a golden model of the waveform that is platform-independent for verification purposes against platform-specific implementations.

Commercial telecommunications waveforms are typically far better specified since there are multiple companies involved in the process, each of which

need to be able to build equipment that can interoperate. This allows anybody to develop compliant radios and compete on the open market—a scenario that could also be applied to the defense industry to reduce costs.

Myth #3: Writing "Generic" Code Is the Answer

Some people would propose writing only generic Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) that does not take advantage of any inherent architectural features of the target FPGA, such as DSP blocks, embedded processors or partial reconfiguration. This generic approach, by its very nature, is inefficient and fails to take advantage of the billions of dollars invested in the semiconductor industry annually. This may work relatively well where size, weight, power and cost (SWAPC) are not particularly onerous constraints. However, this is rarely the case for applications such as tactical radios, particularly small-form-factor and handset radios that rely on batteries.

Because of the rapid evolution of FPGA technology, and the divergence of platform-specific hardware features, development tools currently are not able to abstract the hardware as efficiently as modern C++ compilers can for the case of machine code. Optimizations have to be instantiated at a low level, akin to in-line assembly programming in the software world. In these cases, the executable code is a poor vehicle for reuse. However, if sufficient artifacts exist, including a platform-independent model, it is relatively easy to develop multiple platform-specific implementations that can meet the size, weight, power and cost restrictions of the target deployment platform. Naturally, while developing the platform-specific implementation, it is most efficient to reuse as much existing code as possible without jeopardizing the SWAPC requirements.

Myth #4: Write Once, Run Anywhere Code

One of the early concepts associated with JTRS was that of having a waveform source code base housed in a repository that could run on any radio platform with little to no porting cost—essentially code that can be written once and subsequently run on any platform. This concept was largely based on a general-purpose processing model. Let's examine this myth more closely.

It is certainly true that C code written for a GPP is generally more portable than FPGA code. Why is this? Not only are the instruction set architectures for most GPPs fairly similar but, more importantly, GPPs greatly benefit from having an underlying operating system that abstracts much of the details of the underlying hardware. It is because of this level of abstraction that one can write code that will recompile on, say, both an Intel and a Freescale processor. FPGAs provide additional degrees of freedom to developers by allowing specification of the hardware architecture. This freedom enables FPGAs to deliver orders of magnitude greater performance per watt when tailored to a specific application, but abstraction and portability suffer. On the other hand, it is well known that there is often a very significant level of rework needed when porting an operating system between processors. Why should we expect that a similar level of rework would not occur when porting waveforms on FPGAs?

If we look more closely at GPP software for a real-time embedded system like a radio, it's generally not even true that the code will be 100% functionally and behaviorally identical when compiled to another platform. Features such as the size of the processor data cache, and the size and speed of the external memory, can have subtle impacts that can negatively impact real-time performance.

So let's take a step back and discuss the purpose of code portability. The key goal is to reduce development costs. By focusing on portability and reuse, we are implicitly stating that the act of coding is the most expensive part of a product development program. In our experience, this is not the case. If the specification is clear, the architecture sound, the fixed-point analysis and reference model complete, then the act of coding is relatively straightforward. In general, it is far more efficient, repeatable and less costly

to develop a single platform-independent model and then code as many platform-specific implementations as required for disparate platforms, than have to engage in any reverse engineering. As stated previously, this is not mutually exclusive, but rather is additive to any benefits derived from code reuse.

The Path Forward

Code portability is not a panacea for system development cost reduction. If the name of the game is cost reduction, it is necessary to pass knowledge from the developer to the reuser so that code can be identified for reuse, and other code can be efficiently redeveloped for a different target platform. In order to propagate code portability, the necessary preconditions for success must be put in place. Besides the technical artifacts, there is the necessity for a business model that rewards and enforces code reuse. Figure 2 illustrates a simplified concept of how such a business model might work. This means that in the context of an entire defense program, a business model must be put in place such that code reuse can be supported between companies.

The commercial telecommunications industry has been able to put a model in place that involves relatively open specification and ratification whereby competing companies are incented to keep each other honest. Beyond that, an entire industry has been built upon royalties and cross-licensing of key and valuable IP that can enable advances in waveform development. This provides incentives for companies to continue to invest in R&D not only to capture more value via competitive advantage, but also to successfully engage in cross-licensing, since it is virtually impossible that a single company could single-handedly develop a new waveform that does not infringe on any existing patents. In order for an entire defense program to successfully be able to leverage code reuse, the acquisition strategy must put in place a business model that supports code reuse.

This business model could include NRE to pay for the development both of the radio hardware and waveform software, as well as all the design artifacts. It could also incorporate penalty clauses in the event of non-delivery of any key artifacts during design reviews. Royalty payments for each deployment of the executable waveform software could be built into the cost of the radios to the government, such that the radio vendors would not be punished for using third-party waveform software. Regardless of the model in place, unless it can compensate developers for bearing the cost of writing portable software, it is unlikely that code will commonly be designed for portability between different organizations. ▮▮

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Tech Recon

Multi-Core in Radar and SIGINT

Multicore Trend Enters New Phase

No strangers to multiprocessing concepts, military radar designers are primed to embrace multicore embedded processing. Emerging system solutions help ease the way.

Ian Stalker, Product Marketing Manager
Curtiss-Wright Controls Embedded Computing

The military's transition to the use of multicore processors in embedded systems is entering a new phase. It's a phase where developers of military radars and SIGINT systems are embarking on projects that will employ the new generation of multicore processors. Chip vendors including FreeScale, Intel, AMD, IBM and the latest entrant, P.A. Semi, are taking the approach of eschewing faster clock rates in favor of multicore architectures.

As the feature size of processors has passed the 90 nm mark, processor designers have had to grapple with the hard fact that advances in performance can no longer be achieved mostly on the back of higher clock frequency. For its part Intel hit 1 GHz with the Pentium III in mid-2000. Extrapolating with Moore's law predicts the arrival of 40 GHz processors this summer, which is clearly not happening. The power consumption of modern processors "hit the wall" in recent years with dissipation north of 100W.

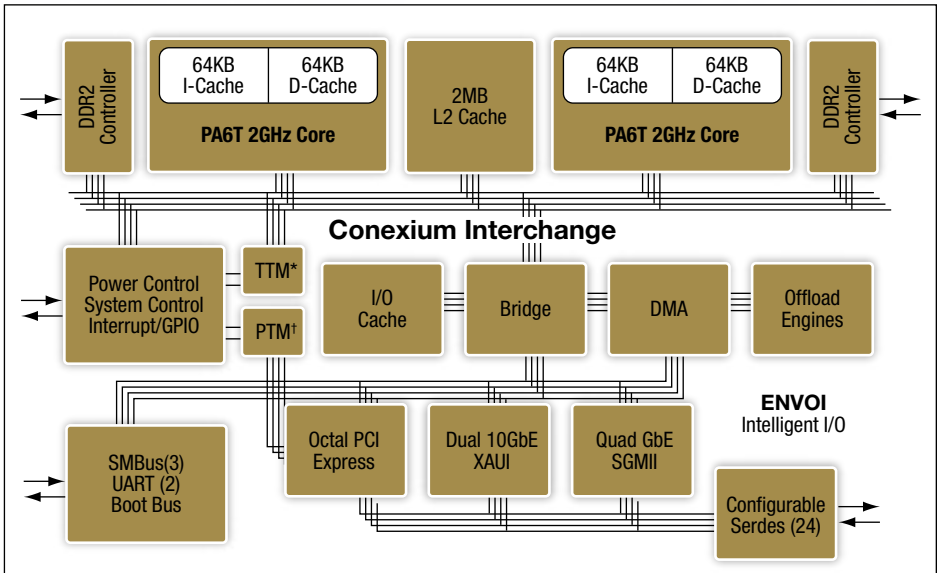

Figure 1

The P.A. Semi 1682 dual-core Power Architecture processor is one of the latest generation of high-performance multicore chips suitable for signal processing algorithms found in radar and signal intelligence applications.

Even in desktop computers with enormous heat sinks, this trend had to stop. Fortunately for the embedded user, multicore processor designers have also been focusing on minimizing power consumption with a variety of energy-conserving techniques. The latest processors from P.A. Semi in particular deliver exceptional performance-per-watt that is the industry benchmark for a high-performance 64-bit processor (Figure 1). Laptops and environmental concerns are driving technology in a direction that is a perfect fit for the size, weight, power concerns that constrain rugged military computers.

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Like it or not, for the foreseeable future, developers seeking to build higher-performance systems will need to harness the power of multiple processor cores working in parallel. The software design challenge posed by these new multicore processors depends on one's starting point. The irony is that relatively simple, single-processor, single-threaded software will potentially require the greatest effort to change. The evolution path for many single-processor applications is via the adoption of a Symmetric Multi-Processing (SMP) operating system. An SMP operating system can dynamically allocate suitably written tasks among the different cores in a processor.

Achieving a performance benefit by moving to a SMP-based multicore processor requires that the programmer think of the elements of the application that can run in parallel, and then design the software with the appropriate threading/tasking so that the SMP operating system can allocate tasks to available cores. This is not a trivial exercise, but a necessary evolution of any software that is going to have a future in the multicore world. Embedded Operating system vendors with SMP-capable products include Wind River (both VxWorks and Linux), Sun, Green Hills, LynuxWorks, Microsoft and various Linux vendors.

Developers of radar and SIGINT systems, however, have a head start on this transition. This is because the majority of these systems have for many years employed multiprocessor architectures. From a hardware perspective, the coming generation of multicore embedded computer boards will provide more FLOPS and interboard bandwidth, while using the same space and similar or less power. Integrators will either consume this computing power to achieve more capability, or some will take the opportunity to reduce the cost and power of legacy systems.

Moving to multicore processors will be an evolutionary change for programmers who are accustomed to distributing a computing problem across many processors. Curtiss-Wright's experience with customers using its dual-core FreeScale 8641-based products is that the large majority of signal processing customers prefer to overtly program each core of a multicore processor, rather than rely on the services of an SMP operating system. Since the problem is still going to involve many separate processor chips connected via a high-speed switched serial fabric, there is little to be gained by having islands of SMP processors. These users are usually seeking to squeeze the maximum performance (and performance-per-watt) from their hardware.

The best approach is to use an Asymmetric Multi-Processing (AMP) software architecture. An operating system running an AMP implementation provides the programmer with two (or more) virtual processors, each with identical CPUs, cache and protected memory regions. There are, however, resources within processors that are intended to be shared between all the cores. For instance, within the highly integrated FreeScale 8641, two cores both have access to a pool of DMA controllers, timers, serial and Ethernet controllers. A well-designed board support package (BSP) will isolate the programmer from the chore of managing these resources by providing allocation, queuing and semaphore functions to control access to shared resources. Figure 2 shows an example of a board sporting four dual-core FreeScale 8641 processors.

Figure 2

Curtiss Wright's CHAMP-AV6 VPX board with four dual-core FreeScale 8641 processors.

Communicating Between Cores

If one's application program is running on a single multicore processor, then the communication between cores occurs via the shared memory (and/or L2 cache depending on the device). In a larger system with more processors, developers prefer a unified communications library where intra-core, intercore and interprocessor messages and data transfers all make use of the same application programming interface (API). The communication library can choose what hardware transport mechanism to employ based on its knowledge of the destination.

Developers have some choices to make on the selection of the communications library, each with attendant strengths and weaknesses. TCP/IP is clearly the "most standard," but until TCP offload engines (TOE) are ubiquitous, it comes with a performance overhead unacceptable to most DSP developers. None of the aforementioned multicore processors have significant TOE features. High-performance libraries such as Curtiss-Wrights Inter-Processor Communications (IPC) library are more proprietary, but strive for speed, low latency and overhead.

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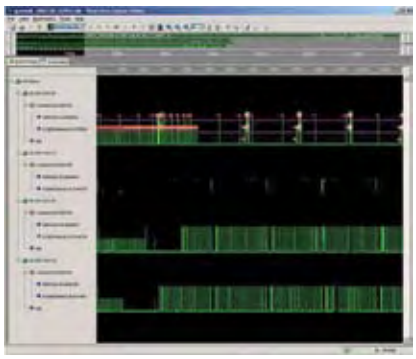

Figure 3

Multicore, multiprocessor debugging is aided with tools such as Curtiss-Wright's Continuum Insights, which can correlate events in time across the entire system. Pictured is the Wind River System Viewer displaying events occurring on four processors simultaneously.

The good news is that multicore processors do not bring a significant new debugging challenge as compared to the current multiprocessor paradigm. The bad news is that this is already hard enough. The vast majority of embedded software debugging tools are designed to support a single processor model. It is certainly true that the software vendors have and continue to evolve their tools for multicore processors. However, once the application program extends past the confines of one chip, most debugger tools are of limited value.

The biggest problem in a multiprocessor system is correlating in real time, software events that are occurring on different CPUs. Curtiss-Wright has taken the approach of extending the capability of standard software analysis tool to make it multicore, multiprocessor, multiboard capable. Curtiss-Wright chose the popular System Viewer tool from Wind River Systems upon which to base our Continuum Insights multiprocessor Event Analysis tool. Insights and System Viewer are used by programmers to record software events of interest in real time, and then use a powerful graphical analysis tool post-runtime to inspect the temporal behavior of a distributed processing application.

Programmers can instrument problematic regions of their code to record events in local memory with very little impact to its real-time performance. In order to present the programmer with a time-aligned view of events across the entire system, the event recording agent relies on a globally accessible, or distributed synchronized time base (Figure 3). Curtiss-Wright has taken advantage of features defined by the VITA 46 (VPX) standard to equip processors with locally readable, but system-wide synchronized timer. This is a relatively simple but very effective technique to assist with challenging multiprocessor debugging.

More of the Same for Radar, SIGINT

For the next few generations of processors, radar and signal processing developers will find that multicore solutions present a similar environment to the current systems constructed with multiple single-core processors. Most will overtly manage the cores as separate virtual processors rather than employ an SMP operating system. However, as processors start to show up with four, eight are more cores, one might envision that software assistance such as SMP may be embraced.

The future looks bright. The major embedded processor suppliers have roadmaps that promise more cores and power-conserving designs, thus providing years of technology insertion opportunities that will not break the traditional multiprocessor software architecture that most radars and signal processing systems are based on. ▮▮

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Tech Recon

Multicore in Radar and SIGINT

Multicore Gaming Tech Boosts Next-Gen Radar

Next-gen airborne radar imaging needs more processing capability while meeting stringent power constraints. Multicore technology addresses the scalability and parallel-programming challenges of these next-generation systems.

Jeffery Rudin, Staff Systems Engineer
Mercury Computer Systems

Airborne Synthetic Aperture Radar (SAR) has been used for reconnaissance in environments where electro-optic and infrared technologies cannot be used such as during the night or when the scene is obscured by weather conditions. SAR provides the warfighter with a flyby snapshot of an area that can be used for terrain mapping, targeting and assessment of troop movement. In addition, because SAR uses coherent processing, it can literally find "footprints in the sand" where the other technologies cannot. Because of the power of today's modern processors, many operations such as these can be performed with a single processor core. However, the mission is changing.

Today's counter-insurgency operations require more than reconnaissance—they require surveillance. The ability to observe an area on a 24/7 basis enables the warfighter to monitor real-time activity and perform forensic analysis. This capability is provided by Circular-SAR (CSAR). Instead of a straight-line flyby, the airborne platform circles the area of observation, continuously illuminating an area with radar. Instead of snapshots, a SAR movie is created, increasing the required processing by the frame rate. This new mission requires much more processing in order to reformat and coherently integrate the radar signals. Additionally, this must be accomplished in the power- and energy-constrained airborne environment.

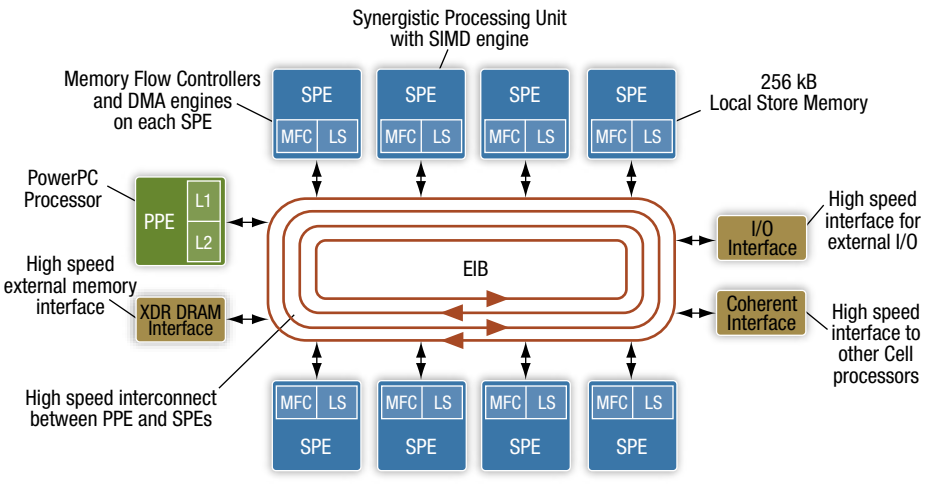

Figure 1

The IBM Cell Broadband Engine (BE) processor offers dramatically improved performance for graphic-intensive workloads and computationally intensive applications.

Multicore processing chips answer the power-energy challenge while increasing processing capability. For many years, increasing the computational power of processing chips has been achieved by increasing the core clock frequency. However, this increases the required input power and cooling by the cube of the frequency. A partial answer is achieved by using superscalar, single-instruction multiple-data (SIMD) architectures and larger memory caches.

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Bus	AT Expansion Bus	✓	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Universal Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓
	PCI Bus Masters	4	4	4	4	4	4	4	4	4	4			4
	APIC (add'l PCI interrupts)	9	9	9	9	9	9	9	9	9	9			
CPU and BIOS	CPU Max Clock Rate (MHz)	1000	1400	1400	1400	400	650	400	650	400	650	333	333	333
	L2 Cache	512KB	2MB	2MB	2MB	256k	256k	256k	256k	256k	256k	16K	16k	16k
	Intel SpeedStep Technology	✓	✓	✓	✓									
	ACPI Power Mgmt	2.0	2.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0			
	Max Onboard DRAM (MB)	512	512	1024	1024	512	512	512	512	512	512	256	256	256
	RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Quick Boot Option Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	EIDE Controller (MB/sec)	100	100	100	100	100	100	100	100	100	100	33	33	33
	ATA/IDE Disk Socket, 32 DIP	4GB	4GB	4GB	4GB	4GB	4GB	4GB	4GB	4GB	4GB	4GB	4GB	4GB
	Audio			✓	✓	✓	✓	✓	✓	✓	✓			
	Digital Video	LVDS	LVDS	LVDS	LVDS			TTL	TTL	LVDS	LVDS	TTL	TTL	TTL
	Analog Video	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA
	AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O	RS-232/422/485 Ports	2	2	2	1	2	2	2	2	2	2	2	2	2
	USB 2.0 Ports	4	4	2	4									
	USB Ports					2	2	2	2	2	2	2	2	2
	10/100Base-T Ethernet	1	1	1	1	1	1	1	1	1	1		1	1
	ECP Parallel Port			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	aDIO(Advanced Digital I/O)	14	14	18	18	18	18	18	18	18	18	18	18	18
	multiPort(aDIO, ECP, FDC)			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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Bus	AT Expansion Bus	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Expansion Bus Master	✓	✓				✓							✓	✓
	McBSP Serial Ports	✓	✓				✓								
Analog Input	Single-Ended Inputs	16	16	16	16	16	16								
	Differential Inputs	8	8		8	8	8								
	Max Throughput (kHz)	1250	1250	40	500	100	1250								
	Max Resolution (bits)	12	12	12	12	16	12								
	Input Ranges/Gains	3/7	3/7	3/1	3/4	1/4	3/6								
	Autonomous SmartCal	✓	✓												
	Data Marker Inputs	3	3		3		3								
Conversions	Channel-Gain Table	8k	8k		8k	8k	8k								
	Scan/Burst/Multi-Burst	✓	✓		✓	✓	✓								
	A/D FIFO Buffer	8k	8k		8k	8k	8k								
	Sample Counter	✓	✓		✓	✓	✓								
	DMA or PCI Bus Master	✓	✓		✓	✓	✓	✓						✓	
	SyncBus	✓	✓				✓								
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	48	18/9	32	64	32	48	48
	Bit Programmable I/O	8	8		8	8	8	8	24	6/0				48	✓‡
	Advanced Interrupts	2	2		2	2	2	2	2					2	
	Input FIFO Buffer	8k	8k		8k	8k	8k							4M	8M
	Opto-Isolated Inputs										16	48	16		
	Opto-Isolated Outputs										16	16			
	User Timer/Counters	3	3	3	2	3	3	3	3	3				10	6
	External Trigger	✓	✓		✓	✓	✓	✓	✓					✓	
	Incr. Encoder/PWM									3/9					✓‡
	Relay Outputs												16		
Analog Out	Analog Outputs	2	2		2	2	2	4							
	Max Throughput (kHz)	200	200		200	100	200	200							
	Resolution (bits)	12	12		12	16	12	12							
	Output Ranges	4	4		3	1	4	4							
	D/A FIFO Buffer	8k	8k				8k	8k							

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Multicore technology takes this trend a step further through the use of multiple full-function cores, each with its own local memory, on a single chip. Surprisingly, the movement toward multicore technology has not been driven by military applications, but instead by the video gaming industry.

A prime example of this new generation of chips is the IBM Cell Broadband Engine (BE) processor developed originally by IBM, Sony and Toshiba for the Sony PlayStation 3 video game console and other consumer electronics devices (Figure 1). The Cell BE is essentially a distributed-memory, multiprocessing system on a single chip. It consists of a ring bus that connects a single PowerPC Processing Element (PPE), eight Synergistic Processing Elements (SPE), a high-bandwidth memory interface to the external XDR main memory, and a coherent interface bus to connect multiple Cell processors together.

The SPE is the heart of the computational capability of the Cell processor. Each SPE incorporates a 128-bit wide SIMD vector processing unit, 128 128-bit general-purpose registers, a 256 Kbyte Local Store (LS) memory, and a Memory Flow Controller (MFC) that controls the DMA transfer of data between the off-chip XDR memory and the on-chip SPE Local Store.

The PPE and the eight SPEs are connected together by the Element Interconnect Bus (EIB) that can transfer up to 205 Gbytes/s. The EIB also connects the processing elements to an XDR memory controller that can provide 25.6 Gbytes/s to off-chip memory, and a 20 Gbyte/s Coherent Interface Bus that permits two Cell chips to be connected for symmetric multiprocessing (SMP).

Modern radar imaging systems require a scalable approach to accommodate the size, weight, power and cooling constraints imposed by various airborne platforms. Configuring a hardware solution around the IBM BladeCenter offers an off-the-shelf solution to this scalability. The resulting optimized solution reduces racks of commodity servers into a single rack with a dramatic reduction in power, space and cost, and with significantly superior performance levels not economically possible before. The system can be configured with up to 28 blades in a 25U rack or up to 42 blades in a 42U rack. External network connectivity is provided via Gbit Ethernet interfaces or optional high-speed fabric connections, including InfiniBand and 10 Gbit Ethernet.

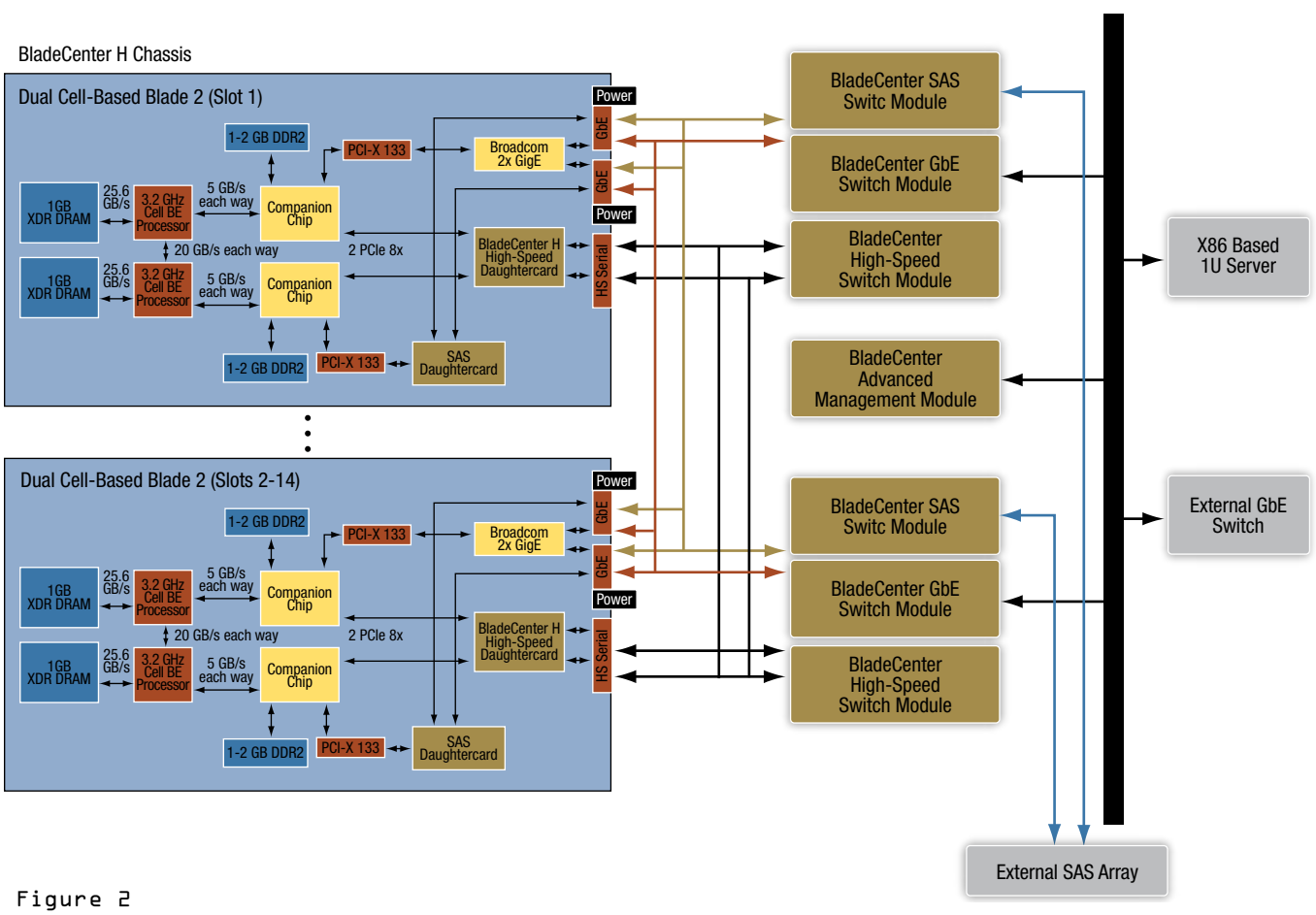

Figure 2

Mercury's Dual Cell-Based Blade 2 is a flexible solution based on the Cell BE processor and the open BladeCenter standard for managed server chassis.

The Mercury Dual Cell-Based Blade 2 (DCBB2) has two Cell BE processors operating in SMP mode with full cache and memory coherency (Figure 2). Each processor running at 3.2 GHz has 205 single-precision GLOPS of performance in the SPE array, for a total of 410 GFLOPS on each blade. The maximum configuration, containing 42 DCBB2 boards, provides 17.2 single-precision TFLOPS of performance in a 42U cabinet, with room to spare for additional support components.

Each Cell BE processor has a "companion chip" that adds rich functionality and high performance to complement the processor. Each companion chip incorporates a high-performance, multi-channel DMA engine with striding and list DMA support. It also includes a low-latency mailbox mechanism for intra-blade event notification between Cell processors. Each companion chip implements 24 lanes of PCI Express with a total sustained theoretical bandwidth to the blade of almost 10 Gbytes/s simultaneously in each direction.

The DCBB2 includes 1 Gbyte of XDR DRAM per Cell BE processor. The XDR DRAM device architecture enables the highest sustained bandwidth for multiple, interleaved randomly addressed memory transactions. In addition, two DDR2 DIMM sockets are attached to each companion chip supporting up to 1 Gbyte DIMMs each. In total, the DCBB2 can support up to 10 Gbytes of memory.

Input/output connectivity is provided by two PCI Express x8 interfaces connecting to a high-speed daughtercard site that can accept cards such as the InfiniBand 4X HCA expansion card, which provides dual 4X InfiniBand to the midplane. In addition, a dedicated Gbit Ethernet controller chip is connected to the dual Gbit Ethernet ports on the BladeCenter midplane.

Parallelized SAR Challenges

Challenges to implementing a parallelized SAR algorithm on the Cell BE include efficiently partitioning and moving the data and tasks across the SPEs while maintaining a high-computational efficiency through the use of efficient-instruction pipelining, register use and exploitation of the SIMD processing engines.

In order to harness the full performance potential of the Cell BE processor, developers need the help of a software framework that supports its computation model and heterogeneous, distributed-memory architecture. The Mercury MultiCore Framework (MCF) middleware provides precise control of fine-grained data distribution and assignment of processing resources on a multicore processor, but relieves them of the hardware-specific details involved. It supports resource allocation and data distribution for the implementation of real-time processing goals. These goals include minimizing, efficient use of resources, overlapping computation and communication, controlling computational granularity and maximizing SPE computational efficiency.

MCF provides a simplified parallel-programming model based on the Data Reorganization Interface. It offers multiple levels of programming that trade off efficiency with programming simplicity. This permits implementers to focus on those parts of the algorithm with the highest value. It provides this multi-level support through the use of high-level data channels that simplify data distribution and reconstitution, and lower-level functions such as message queues, barriers, semaphores and DMA instructions that permit direct transfer of data between SPE Local Store memories without going through XDR. MCF also provides functions to allocate data buffers that are aligned to the memory in order to achieve optimum DMA performance.

Tested for SAR Use

To test the applicability of the Cell BE to SAR, key components of SAR algorithms such as interpolation, corner-turns and range and azimuth compression were selected for parallelization. It should be noted that the interpolation algorithm performs non-uniform 2D coherent interpolation that can dominate the processing cycle. For this reason, the implementation

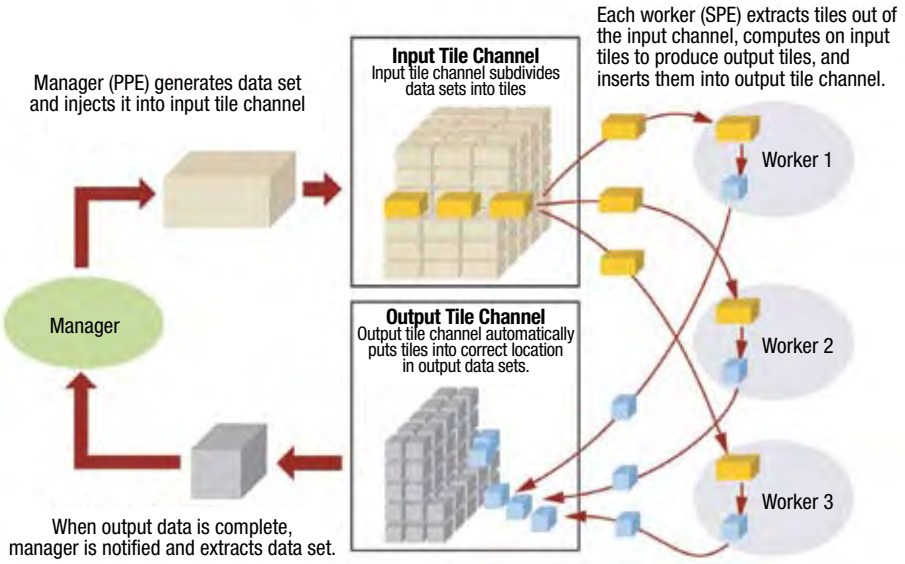

Figure 3

In the Multicore Framework, tile channels facilitate the communication and data movement between the manager and the workers for lower latency and efficient resource utilization.

of the interpolation algorithm was the particular focus of this effort.

The parallelized SAR algorithms were implemented using a "function-offload" programming model, where the PPE acts as a manager directing the work of the SPEs. Sections of the algorithm were loaded into the SPEs as individual "tasks." Input frames residing in XDR memory were divided into "tiles" and distributed to the SPEs where they were processed using the "tile channel" construct (Figure 3). The tile channel automatically partitions and synchronizes the scatter-gather dataflow between the main XDR memory and the SPEs' Local Store memory. Processed tiles were then gathered back to the XDR memory using a return channel.

In general, there is a one-to-one relationship between the input and output tiles, which results in a simple get-tile/put-tile loop being executed on each SPE. Parallelization of the algorithms also required the data tiles to overlap by 12.5%; this was easily accomplished using the built-in overlap feature of the tile channel. (Essentially, the parallelized version had to process 12.5% more data.) Utilization of the SPEs was maximized by minimizing the number of trips the data had to take to the XDR memory.

These algorithm benchmarks were then run for various image sizes and numbers of SPEs to examine scalability. The image sizes were varied independently in both range and azimuth. The results showed a high degree of linear scalability of the algorithm both with the size of the problem and the number of SPEs dedicated. When compared to a non-parallelized algorithm implemented on a single-core 500 MHz PPC, the parallelized algorithm ran 42x faster and was 3x more energy efficient on the 3.2 GHz Cell processor, clearly showing the advantages of multicore processing. ■■

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PC/104 Tightens Ties Between Board and Box-Level Computing

As the military continues to shift its demand toward complete stand-alone rugged box-level systems, PC/104 is closing ranks as the dominant expansion form-factor in those solutions.

Jeff Child,
Editor-in-Chief

The list of military programs using PC/104 in the airborne, marine, handheld and vehicular arenas continues to lengthen. Military system developers select PC/104—and its wider community of form-factors including PC/104-Plus, PCI-104 and EPIC—because of its compact size as well as the ruggedness inherent in its stacking architecture. Many of those applications require a certain degree of sophistication when it comes to electronics enclosures and packaging. That's particularly the case for applications with demanding environmental specifications where the system is tasked to operate reliably in harsh field conditions.

Certainly the lack of a backplane and the use of a pin-and-socket mating connector naturally help make PC/104 inherently rugged. That said, dealing with heavy loads of shock and vibration energies, submergence in seawater, extreme temperature operation or electromagnetic pulses (EMP) make a sound mechanical design for PC/104 systems all the more critical. This stacked multiboard system provides for a shock- and vibration-resistant off-the-shelf computing solution by eliminating backplanes and metal card cages, making PC/104 ideal for military vehicles such as tanks or even Humvees. Crafted especially for military program requirements, a growing assortment of semi-custom PC/104 enclosure and chassis solutions has been available from several PC/104 vendor companies.

Figure 1

The Expeditionary Fighting Vehicle (EFV) replaces the Marine Corps' Amphibious Assault Vehicle (AAV). Using an onboard router implemented with a PC/104-based DuraMAR system, the EFV will help the Marines sustain inland combat operations and providing on-the-move command, control, communication and computer intelligence (C4I) capabilities.

Within the past year or so that trend has advanced to where these "stand-alone" box-level computers with PC/104 inside are now part of many vendor's product lines, rather than just a pure custom solution. This fits in with the broader trend where traditional embedded board vendors are adding stand-alone rugged box-level systems to their military market offerings. These complete system boxes—which often support standard form-factor boards inside them—provide a complete, tested and enclosed computing solution that eliminates complex integration chores for customers. The systems typically comprise a set of modular embedded boards housed in a rugged enclosure that has its own power supply and interface ports to link to a variety of user terminals.

An example along those lines is the DuraCOR 810 from Parvus. It's a rugged tactical computing platform integrating a low-power 1.4 GHz Pentium-M processor and PC/104 card expansion slots. The Naval Surface Warfare Center (NSWC) chose the DuraCOR 810 processor systems and DuraMAR 1000 mobile routers for use with the Navy's Littoral Combat Ship (LCS) program. The DuraMAR router is also used in design of the Tactical Switch Router (TSR) for the United States Marine Corps' Expeditionary Fighting Vehicle (EFV) (Figure 1). The TSR router is based on Parvus' DuraMAR Mobile IP router product, a rugged router system integrating Cisco System's 3200 Series Wireless and Mobile Router technology. The Tactical Switch Router enables the deployment of communications-on-the-move and information-sharing capabilities, supporting the Marine Corps' net-centric operations initiatives.

The Navy's newest class of surface warship, the LCS operates manned and unmanned vehicles (UVs) for conducting mine warfare (MIW), anti-submarine warfare (ASW) and surface warfare (SUW). Two DuraCORs and one DuraMAR unit are specified as part of the communications equipment package for each LCS Unmanned Surface Vehicle (USV) being developed to carry out these warfare missions.

Figure 2

Octagon Systems' XMB Mobile Server lets system designers mix and match I/O and other functions via PC/104 add-in cards. The basic unit includes the processing power, power supply, memory and I/O for most applications. Additional I/O such as GPS, analog, GPRS and video camera can be readily added via PC/104, PC/104-Plus and XBLOK modules.

Also exemplifying the marrying of stand-alone rugged boxes and PC/104 is Octagon Systems' XMB Mobile Server product (Figure 2). The drawback to a complete all-in-one system has always been the lack of flexibility to customize to application requirements. With that in mind, Octagon Systems nullified that drawback by offering a product that marries the complete system approach with the ability to mix and match I/O and other functions via PC/104 add-in cards. The basic unit includes the processing power, power supply, memory and I/O for most applications.

Standard I/O includes dual Ethernet, quad USB 2.0, dual serial, CRT and LCD video and digital I/O. Because the XMB-1 is fully functional out-of-the-box, additional I/O such as GPS, analog, GPRS and video camera can be readily added via PC/104, PC/104-Plus and XBLOK modules. An option panel can be easily removed and punched for custom annunciators, connectors and controls. Generated heat is efficiently channeled directly to the case to help prevent internal hot spots. The XMB Mobile Server operates in ambient temperatures from -40° to 75°C, depending upon the processor speed, user options and mass storage devices.

New Rugged Box Solutions

The stand-alone rugged box trend has opened up a whole set of product choices for military system designers. To date many such systems have been on the expensive side. Offering a low-cost (sub-$1,000) alternative, Adlink Technology offers its compact PC-based controller system. The GEME-42000 from Adlink Technology is equipped with an Intel Ultra Low Voltage Celeron M processor (1.0 GHz) and up to 1 Gbyte of DDR333 RAM, and can be controlled from remote locations and run continuously in mission-critical applications.

The GEME-42000 meets the needs of embedded controllers; it is compact, has front side access, is highly reliable and offers an expandable architecture with optional motion, I/O and communication modules in PMC or PC/104 form-factors. Power supply options include standard AC power for stationary applications and DC power for mobile applications such as in vehicles.

Much debate continues in the industry as to whether the venerable ISA-bus is worth supporting. Even given the long design cycles of military programs, ISA has moved far beyond its prime. In the PC/104 universe, leaving ISA behind translates as the PCI-104 flavor of PC/104. PCI-104 maintains the PC/104 mechanical form-factor, but includes only PCI while omitting the 104 connector that supports ISA.

Advantech has added a new compact embedded computer to its ARK-4000 product series that's based on PCI-104. The ARK-4180 (Figure 3) features high vibration/shock resistance and wide temperature capability. The ARK-4180 with Intel Celeron M 1.0 GHz processor can operate in temperatures ranging from -40° to 75°C, providing high processing performance in a compact, rugged enclosure. The ARK-4180 is developed from PCI-104 stackable modules. The PCI-104 form-factor allows modules to stack vertically to provide a naturally rugged architecture. Each system is housed in a specially cast and milled solid aluminum block with thermal fins that help dissipate heat.

Figure 3

The ARK-4180 is developed from PCI-104 stackable modules. The PCI-104 form-factor allows modules to stack vertically to provide a naturally rugged architecture.

Another feature is the specially designed fanless thermal solution with embedded heat pipes, which allow wide temperature operation without active cooling. The ARK-4180 supports six USB 2.0 and two RS-232 connectors, 10/100Base-T Ethernet LAN and VGA for versatile connectivity. It supports one PCI-104 connector for expansion, and by adding another enclosure layer, up to two more PCI-104 modules can be stacked.

The "EPIC" Struggle

Designed as an upgrade path from PC/104, perhaps the most significant news to spring from the PC/104 community was the roll out a couple years ago of the Embedded Platform for Industrial Computing, or EPIC, form-factor. The EPIC spec was developed jointly by a cross section of major PC/104 players. The EPIC form-factor fills the need for a mid-range-sized form-factor between that of PC/104 and the EBX motherboard

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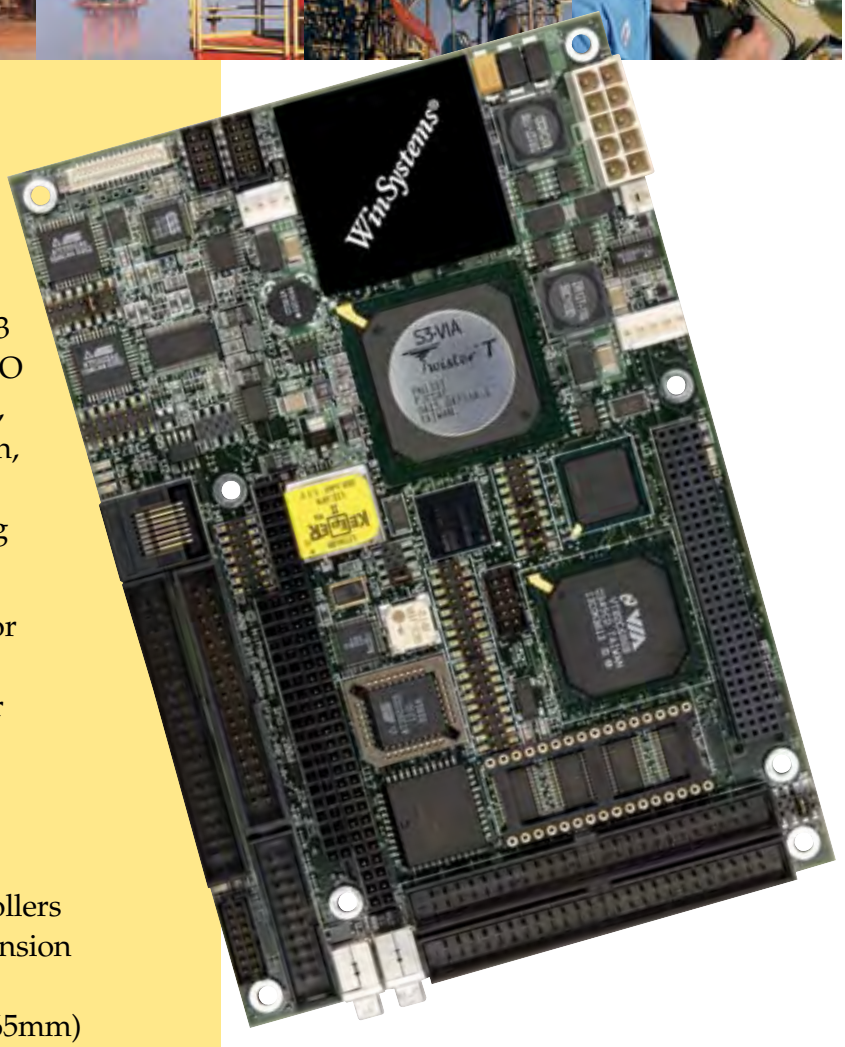

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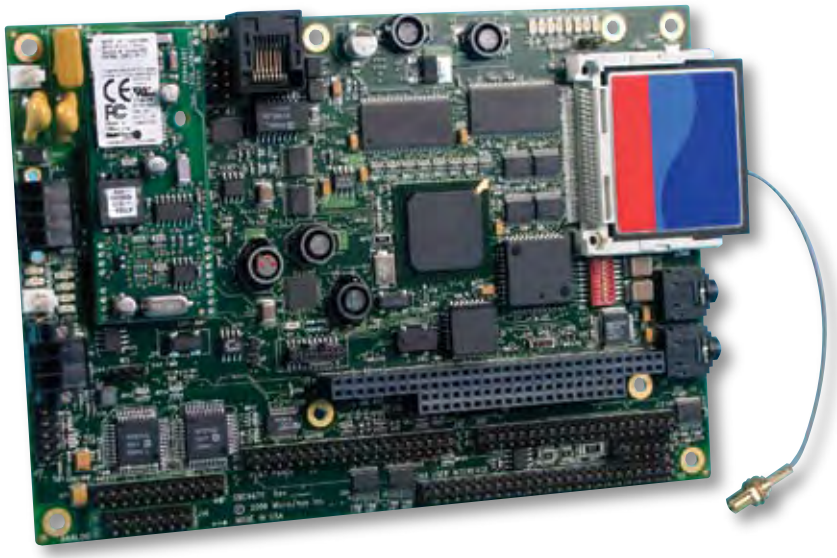

Figure 4

The EPIC form-factor SBC4670 from Micro/sys combines the fast, low-power 520 MHz PX270 ARM processor with Power Over Ethernet, onboard GPS, a socket modem capable of GSM/GPRS, CDMA or Bluetooth, and/or a CAN bus interface.

standard. The same group of vendors that created the EPIC form-factor followed up with the publication of the EPIC Express Specification, which adds high-bandwidth PCI Express I/O expansion to EPIC form-factor SBCs. Most of these vendors offer both PC/104 and EPIC families of products. Unfortunately connector issues have held back EPIC Express's progress. A number of vendors have rolled out new EPIC SBC products in the past twelve months, including Arcom, Diamond Systems, Octagon Systems and Micro/Sys.

In many applications ratcheting down the amount of power consumption in a subsystem is a priority. That's why Arcom designed its ZEUS EPIC-sized SBC to consume only 2W typical. Combined with dynamically adjusted sleep modes, extensive communications options, a wide operating temperature range and a vehicle-compatible power supply, the board's ultra-low-power design makes it ideal for vehicle tracking, mobile terminals and network communications controllers.

The RoHS-compliant board is based on the Intel 520 MHz PXA270 XScale RISC processor. ZEUS has seven onboard serial ports to support a wireless modem and GPS and provides traditional hardwired serial I/O functions for legacy communications. A small adapter module fitted with a variety of GSM/GPRS, iDEN and CDMA wireless modem modules is optional. The board includes up to 256 Mbytes of soldered SDRAM and up to 64 Mbytes of soldered AMD MirrorBit flash. 256 Kbytes of battery-backed SRAM using the onboard battery are provided.

Other features include a TFT/STN flat panel graphics controller, analog touch screen controller, dual 10/100BaseTx Ethernet ports, I^2C controller, dual USB host controller, USB client, AC97 audio/codec, CompactFlash interface, SDIO and a standard PC/104 bus expansion connector. The ZEUS may be powered from the integrated DC/DC PSU (10-30V) or from a single +5V input. The power supply has been designed for use with vehicle power looms and features transient suppression and protection.

With a Data Acq Spin

On a single board, the Poseidon EPIC form-factor SBC combines the VIA Eden ULV or VIA C7 processor running at speeds of up to 2 GHz with Diamond Systems' patented, automatically auto-calibrating A/D circuitry. The connector board is removable, providing pin headers for a more rugged interface.

The Poseidon includes 256 Kbytes of on-chip cache, a 400 MHz front-side bus and up to 512 Mbytes of onboard soldered 533 MHz DDR2 RAM. The VIA CX700 integrated digital media chipset integrates the VIA UniChrome Pro 2D/3D graphics controller with integral MPEG-2 hardware acceleration, CRT and LVDS flat panel support, and dual independent display capability. The Poseidon SBC also provides four USB 2.0 ports, two RS-232 ports, two RS-232/422/485 ports, IDE and SATA hard drive interfaces, and an Intel 82541 Gigabit Ethernet controller. Typical power consumption is under 10W.

For military applications that depend on remote terminals, protocol conversion or data logging in power-shy environments, the ideal SBC would combine a low-power CPU with lots of onboard communications formats. That's exactly what the EPIC form-factor SBC4670 (Figure 4) from Micro/sys offers: it matches the fast, low-power 520 MHz PX270 ARM processor with Power Over Ethernet, onboard GPS, a socket modem capable of GSM/GPRS, CDMA or Bluetooth, and/or a CAN bus interface. The board also contains support for an 800 x 600 color flat panel display, audio output and debounced keypad input, as well as eight channels of 14-bit A/D with simultaneous reads, eight channels of 14-bit D/A and 24 channels of digital I/O.

The SBC4670's processor can dynamically shift velocity in response to performance or power consumption changes. On-chip cache, an SDRAM controller, a CompactFlash interface and a USB host controller are also on board, as well as five serial ports, 128 Mbytes of SDRAM, 64 Mbytes of boot flash and a 16-bit PC/104 bus interface. The SBC4670 supports Linux, Windows CE and VxWorks. A stackthrough version is available for plugging into a custom OEM I/O card.

Focus on SWAP

In many defense and aerospace platforms, size, weight and power (SWP) are critical design considerations. Developed for applications that need all three, Octagon Systems offers the EPIC form-factor XE-900 SBC, designed to operate in harsh, demanding environments. The XE-900 incorporates the 32-bit, low-power VIA Eden ESP CPU family. Three versions are

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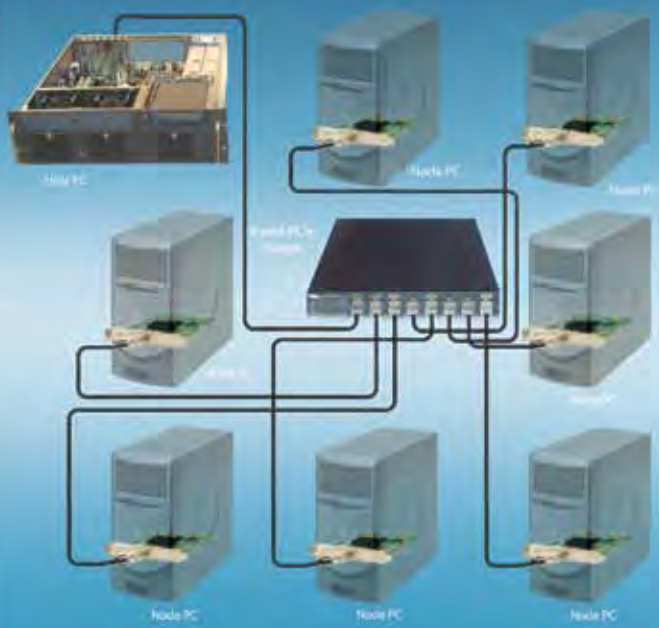

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available: the 400 MHz and 733 MHz versions operate at -40° to +85°C and the 1 GHz version operates at -40° to +75°C.

Memory includes 512 Kbytes of surface mount flash for BIOS, a SO-DIMM socket for up to 512 Mbytes of SDRAM and 1024 bytes of user-available serial EEPROM. ATA-4 hard drive and CompactFlash interfaces support up to three drives: CD-ROM, hard drive, EIDE flash drives and other EIDE devices. The board includes CRT and flat panel video, six RS-232/422/485 serial ports, two USB ports, 10/100 Base-T Ethernet, PC/104 and PC/104-Plus expansion and 24 lines of bit-programmable, digital I/O with 16 mA sink/source capability. It features ACPI 2.0 and PCI power management. The conduction-cooling system eliminates the need for a fan even at 1 GHz. ■■

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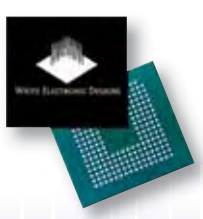

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Technology Focus

FPDP and Serial FPDP

FPDP and Serial FPDP Build on Their Success

Parallel and Serial FPDP continue to hold a solid position for high-bandwidth, low-overhead data movement applications. They shine where simplicity rules and the more complex fabric and network technologies fall short.

Jeff Child
Editor-in-Chief

The Front Panel Data Port (FPDP) and its newer counterpart Serial FPDP offer a simple, low-overhead interface scheme for high-bandwidth, point-to-point data transfers. Implemented with a low-cost ribbon cable, FPDP links boards without eating up more than a tiny amount of board space. Because FPDP does not require a host computer at the sensor end, processing overhead is reduced to the bare minimum, allowing for maximum data throughput. Even better, the elimination of the host computer means no operating system. With all that going for it, FPDP has proven itself as an effective solution for high-throughput, point-to-point data movement.

FPDP is particularly attractive in military applications like radar and sonar where it's used to interface to sensor networks. Because FPDP operates independently of the backplane bus, it provides a deterministic sustained bandwidth free from contention. Meanwhile the more recent FPDP II version provides data rates up to 400 Mbytes/s and has found some acceptance even though it's not an official standard.

The grandchild of FPDP is the relatively young Serial FPDP (ANSI/VITA 17.1-2003) interconnect scheme. Serial FPDP overcomes a key limitation of parallel FPDP: its distance limitations. It does so by using a serial interface based on the Fibre Channel physical layer. Serial FPDP retains the frame format of the original standard thus simplifying the exchange of data between parallel and serial implementations. By doing so, Serial FPDP makes it easy to exchange data from local chassis and legacy systems using parallel interfaces to remote chassis through a Serial FPDP connection. The ANSI/VITA 17.1-2003 specification for Serial FPDP supports 1 Gbit/s, 2 Gbit/s and 2.5 Gbit/s link speeds.

In a typical Serial FPDP setup, parallel FPDP data is converted to Serial FPDP on the transmit side. And then, on the receive side, Serial FPDP data is converted back to parallel FPDP. FPDP data made up of 32-bit words flow through a transmit FIFO to an 8B/10B encoder. Data is then serialized and sent over a fiber or copper wire. Data is deserialized on the receive side, then decoded and sent to receive FIFOs and delivered as FPDP output data.

Figure 1

FPDP is popular in sonar upgrade programs like the NSSN sonar transmit system and NSSN Simulation/Stimulation system (Sim/Stim) aboard their Virginia Class Attack Submarines, like the USS North Carolina. The vessel is shown here in December last year heading out for its first set of sea trials. The North Carolina is scheduled to be commissioned in May of this year.

Serial FPDP uses as little as one percent of a host processor's or FPGA's resources. In contrast, PCI Express, for example, can eat up as much as 40 percent. The addition of an optical connection to the physical layer provides better noise immunity and extended range with distances of up to 10 km being supported by the standard. Future versions of the protocol will support data rates of up to 10 Gbits/s and will be standardized as ANSI/VITA 17.2.

Among the publicly announced wins for FPDP are a number of major sonar upgrade programs, such as sonar for the New Attack Submarines (NSSN). FPDP is used in both the NSSN sonar transmit system and NSSN Simulation/Stimulation system (Sim/Stim) aboard their Virginia Class Attack Submarines, like the USS North Carolina (Figure 1). Other programs using FPDP include the SQQ-89 sonar upgrade for the guided missile (DDG) class of destroyers and the P3 Aircraft. The SQQ-89 sonar transmit and receive systems are used on Arleigh Burke Class (Aegis) Guided Missile Destroyers. ■

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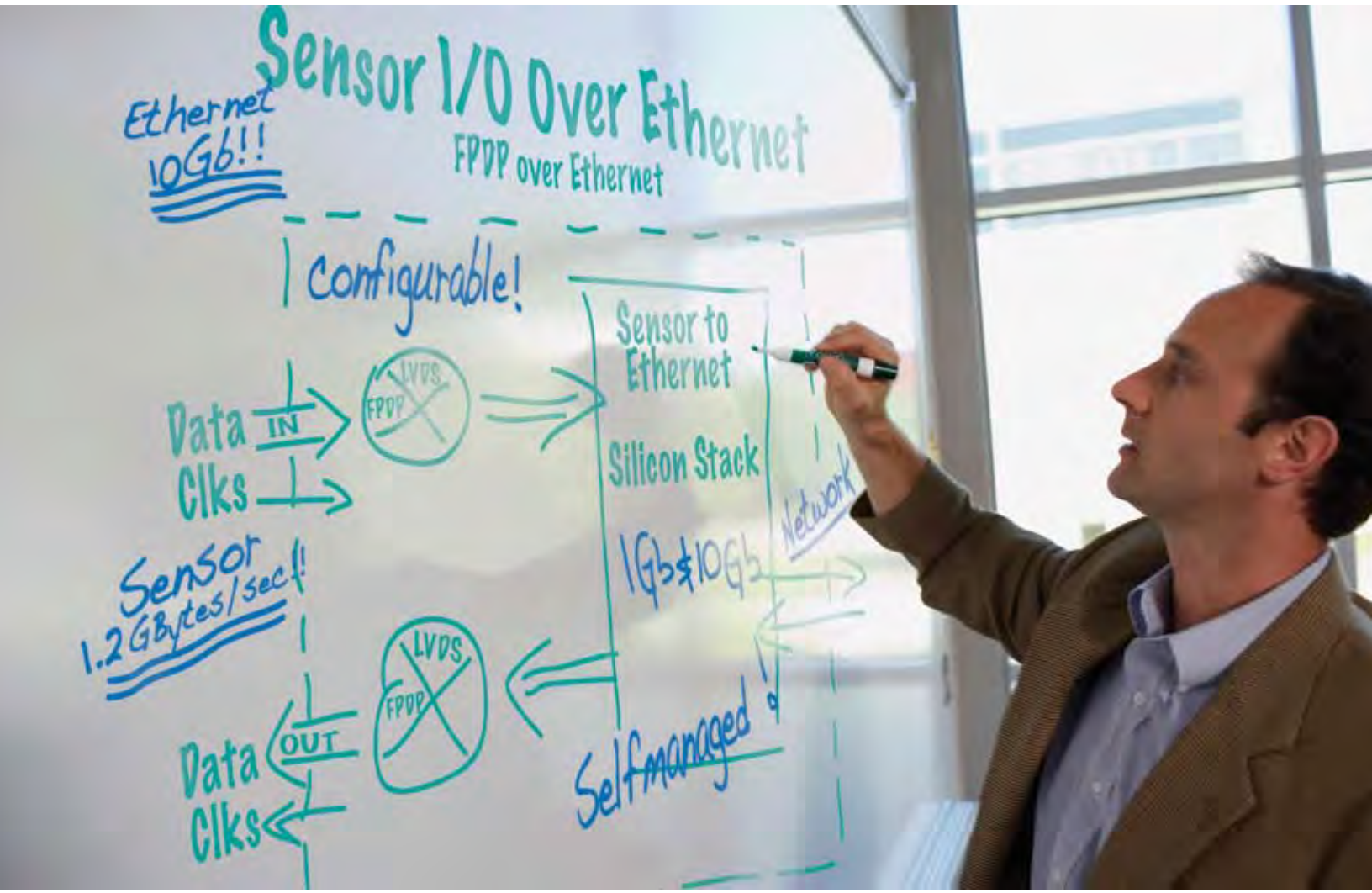

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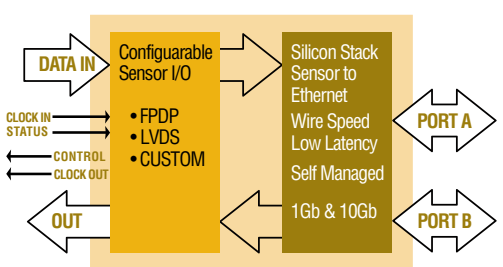

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Technology Focus:

FPDP and Serial FPDP Boards Roundup

Card Serves Up 24 sFPDP Channels per VME Slot

Using FPGAs in conjunction with the Serial FPDP interconnect makes for a power combination. Such a solution has enormous benefits for radar, sonar, SIGINT, ELINT, digital signal processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing and other processing-intensive applications. Serving exactly that arena, Annapolis Micro Systems offers its FPGA-based WILDSTAR family that provides 24 sFPDP channels per VME slot. The Annapolis sFPDP Cards (UNI3 or UNI6) come with an easy to use Serial FPDP interface supporting up to 12 lanes of 2.5 Gbit Full Duplex data. Three frame types are supported: Normal Data Fiber Frame, Sync without Data Fiber Frame and Sync with Data Fiber Frame in Point-to-Point Mode. The card has three individually configurable, industry-standard 4X connectors, providing 4 lanes per connector, with dedicated signal conditioners to ensure clean communication. It supports up to 7.5 Gbytes/s full duplex per I/O card and a wide variety of readily available copper and fiber cables.

Up to two serial I/O cards and two LVDS I/O cards can reside on each WILDSTAR 4 or WILDSTAR 5 VME/VXS main board, with half that number for the PCIX or PCIe. The sFPDP card (UNI6) also supports Rocket I/O protocol at up to 75 Gbit Full Duplex per I/O card, three ports of 10G Full Duplex InfiniBand per I/O card or 10G Full Duplex Ethernet per I/O Card. No other FPGA board vendor can match the volume of data we can send straight into the heart of the processing elements and then straight back out again. WILDSTAR 4 for PCI boards starts at about $13,500 and UNI6 I/O Mezzanines start at about $4,500.

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Board Boasts 3.125 Gbits/s on Four Ports

It's not always possible to get data conversion gear close to where the analog data is acquired. Serial FPDP is rapidly becoming the interconnect of choice for streaming data capture systems because it is a protocol optimized for maximum data rates and minimum overhead. It efficiently accommodates many applications requiring great distances between the data input site and data processing stations. Along those lines, Conduant offers its StreamStor Serial FPDP Mezzanine Board for long-distance, high-speed, data capture from Serial FPDP or other optical fiber data protocols. When combined with Conduant's StreamStor Amazon SATA disk controller, real-time data input performance exceeds 500 Mbytes/s.

The StreamStor Serial FPDP Mezzanine Board features four independent optical fiber interface ports for simultaneous data input and output available on each port. With data rate and wavelength options, the board can support cable lengths up to 25 kilometers. The StreamStor Serial FPDP Mezzanine Board exceeds the ANSI/VITA 17.1-2003 specification with sustained rates of 300 Mbytes/s (3.125 Gbytes/s). Wavelength options include 850 nm (nanometers) and 1300 nm for distances up to 25 kilometers. Data rates range from 1.06-3.125 Gbits/s on each of the four ports. The mezzanine board supports multiport recording whether bonded or independent. It is field-upgradeable and features customizable hardware.

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XMC Does Wide-Band Sensor I/O over Ethernet

The military has warmed completely to the idea of using Ethernet as high-performance interconnect technology. Its ubiquity and longevity make it hard to resist. Applying Ethernet to wide-band sensor I/O, Critical I/O has announced SensorLink, a board-level solution that allows wide-band sensors to be easily connected to, and managed over, 1 Gbit and 10 Gbit Ethernet networks. SensorLink enables system designers to implement an Ethernet "Sensor Fabric" for high-performance systems. The FPGA-based board is a fully self-contained sensor-to-10 Gbit Ethernet bridge. It bridges multiple parallel sensor data ports—that can be configured as industry-standard parallel FPDP and FPDP II, high-speed parallel LVDS, or PCIe—to standard 1 Gbit or 10 Gbit Ethernet, without the need for any host processor at the sensor.

With SensorLink, Ethernet data networks can be applied to even the most demanding real-time applications such as radar, data acquisition, sonar, FLIR, SIGINT, video distribution and signal processing. Completely self-contained and requiring no host processor, SensorLink allows sensor data to be streamed at wire speed with very low latency to other devices connected to the Ethernet network such as signal processors, workstations, storage devices or other SensorLink devices. SensorLink also greatly simplifies the management of sensors by allowing remote processors to configure, control and monitor them through the same Ethernet connection without interrupting the sensor's real-time data flow. SensorLink allows system developers to directly leverage standard Ethernet networks without investing many man-years in software and compatibility testing.

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Rugged Serial FPDP Board Sports Quad Channels

The Serial Front Panel Data Port (sFPDP) interconnect has become the industry standard for high-speed serial communication in today's advanced sensor-to-DSP systems. For its latest sFPDP offering, Curtiss-Wright Controls Embedded Computing has introduced a new rugged, high-performance, quad channel Serial FPDP card that delivers sustained data rates up to 247 Mbytes/s on each of its four channels. The new FibreXtreme SL100/SL240 Serial FPDP card, based on Altera's Stratix II GX FPGAs, connects distributed devices through a highly specialized communications protocol (VITA 17.1-2003) optimized for maximum data throughput. The Stratix II GX FPGA is used to obtain full throughput rate on all four sFPDP channels while providing a full rate PCI Express host bus interface. The embedded transceivers in the FPGA support data rates in excess of 6 Gbits/s, enabling future performance enhancement.

The cards, available in both PCI and XMC mezzanine formats, are designed for use in applications that require high data rates such as digital signal processing, radar and sonar, medical imaging, range and telemetry systems. The sFPDP card off-loads the host processor, enabling data transfers to occur without the CPU overhead and non-deterministic latencies associated with many layers of complex software protocols. Availability of the FibreXtreme SL100/SL240 card is off-the-shelf in the first quarter this year.

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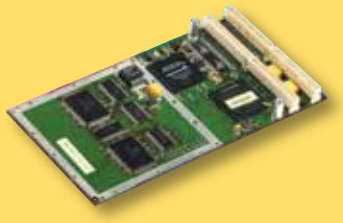
(703) 779-7800.
[www.cwcembedded.com].

Rugged PMC Serves Up FPDP II

Demand is on the rise for multichannel, high-rate sensor data transfer across a single backplane. Providing a solution, GE Fanuc Embedded Computing offers the ICS-8500, the first PMC to become available that delivers 400 Mbyte/s FPDP II—compared with 160 Mbytes/s for FPDP—in a rugged environment. The ICS-8500, which can be configured as either a transmitter or a receiver, also features 8 Mbytes of swing buffer memory, setting it apart from products that provide only limited FIFO capability.



Available in convection- and conduction-cooled versions, the ICS-8500 offers similar functionality to the popular ICS-500-R and ICS-500-T PMC products, but is configurable under software control as either a receiver or transmitter. The 400 Mbyte/s FPDP II interface is provided via the P4 connector: when the ICS-8500 is communicating with a non-FPDP II device, it automatically reverts to ANSI/VITA 17 FPDP operation at 160 Mbytes/s.

In transmit mode, the board provides an FPDP/TM interface. In addition to a continuous data transmit capability, a Loop mode of operation is available, in which a fixed length of data equal to the programmed buffer length is written to both banks of the swing buffer. When triggered, this data is repetitively generated and transmitted by the FPDP output interface. In receive mode, the board provides both Receive (FPDP/R) and Receive Master (FPDP/RM) capabilities. A key feature of the product is its ability to perform the corner turning function: this software-enabled feature reorders multichannel data from channel ordering by time to time ordering by channel.

GE Fanuc Embedded Systems
Albuquerque, NM.
(505) 875-0600.
[www.gefanucembedded.com].

XMC Delivers Two Serial FPDP Channels

Mercury Computer Systems' Sensor I/O XMC daughtercard provides a direct interface into the RapidIO switch fabric for sensor input, enabling low-latency processing of data streaming directly from sensors. The daughtercard implements the Serial Front Panel Data Port (Serial FPDP) protocol over fiber on two 2.5 Gbaud full-duplex channels.

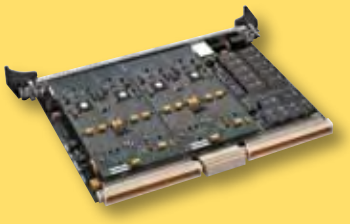
Full system performance is enhanced because each channel can be programmed for data distribution without processor intervention. The interface can sense signals in the data stream that indicate sensor mode changes, and route data appropriately to different processors or endpoints on the RapidIO switch fabric. The board supports connections up to 150m and a real-time latency as low as 4 microseconds. All four FPDP data modes are supported, and it provides four DMA engines with chaining and branching. Support for Serial FPDP is as specified by VITA 17.1-2003 and is compatible with all products supporting any subset of the VITA 17.1-2003 protocol.

The Sensor I/O XMC is software-compatible with RACE++ Series RINOJ-F products, easing migration from the legacy I/O daughtercards while offering significant improvements in speed as well as configuration flexibility. The card draws approximately 6.5W of power (typical) and operates over temps of 0° to 40°C and at altitudes of 10,000 ft. A rugged version of the product is also available.

Mercury Computer Systems
Chelmsford, MA.
(978) 256-0052.
[www.mc.com].

VME Card Blends Serial FPDP and RACE++

For military sensor signal processing systems, acquiring and transmitting data in real time is of critical importance. Meeting those needs, the MM-6467D from Micro Memory has four 2.5 Gbit/s VITA 17.1 Serial FPDP channels, up to 8 Gbytes of memory, dual RACE++ ports, a PowerPC processor and VME interface. The four Serial FPDP channels can each run concurrently at the maximum bandwidth of 247 Mbytes/s per port, with an aggregate bandwidth of almost 1,000 Mbytes/s.



Using a proprietary FPGA windowing implementation on the PCI memory nodes, multiple Serial FPDP channels can DMA data into a single PCI memory node while a DMA from the RACE++ fabric is simultaneously occurring into that same memory node. Serial FPDP channels are tightly coupled to large memory arrays on dedicated PCI bus segments for maximum performance between I/O streams and onboard buffer memory. A transparent PCI-to-PCI bridge separates the two Serial FPDP channels and memory controller from its mirrored pair to enable simultaneous, concurrent bandwidth while providing full connectivity between all devices. The board's 350 MHz PowerPC processor has 128 Mbytes of local SDRAM, up to 32 Mbytes of contiguous direct-mapped flash, and a hardware flash write-protect switch for high-security environments. Other features include a DUART RS-232 serial port, programmable watchdog timer, Real-Time clock and RTC alarm, COP/JTAG and front panel LED status indicators.

Micro Memory
Chatsworth, CA.
(818) 998-0070.
[www.micromemory.com].

Digital Receiver for Software Radio Rides VME

Developers of real-time DSP and software radio systems often want to avoid the lengthy, complex programming that can accompany the use of FPGAs. With the GateFlow Model 6821-422 high-speed A/D digital down-converter (DDC) board from Pentek, now they can. The board includes a factory-installed wideband digital down-converter FPGA IP core operating at frequencies of up to 296 MHz. It is a highly optimized, dual-channel version of Pentek's GateFlow IP Core 422 tailored to the board's various resources. The result is a preconfigured, fully tested digital software radio subsystem that accepts a front-panel analog RF input and delivers real or complex digital output samples translated to baseband from any frequency slice of the input signal. The board has a 12-bit sample rate at 215 MHz and four sets of user-programmable FIR coefficients for custom filtering.

The digital output signals are available on two or four FPDP connectors using several data-packing modes. In addition, the signals can be delivered as low voltage differential signaling (LVDS) through either the VMEbus P2 connector or a second-slot front-panel mezzanine. The Model 6821-422 is supported by Pentek's C-callable ReadyFlow Board Support Libraries. ReadyFlow provides development tools for quick startup through application completion, allows programming at high, intermediate and low levels to meet various needs, and includes complete source code for all functions. Ruggedized and conduction-cooled versions of the board are available. Pricing starts at $17,495.

Pentek
Upper Saddle River, NJ.
(201) 818-5900.
[www.pentek.com].

Serial FPDP PMC Works with Any Protocol

There's no doubt that FPGAs open up a treasure chest of flexibility for designers of I/O subsystems. Using FPGAs, designers can facilitate dropping in blocks of pre-integrated signal processing cores, thereby leveraging single hardware architecture across multiple applications. Following exactly that road, TEK Microsystems came out with the JazzFiber PMC, the first protocol-agnostic fiber-optic PMC I/O module optimized for both streaming I/O and signal processing applications. The JazzFiber Quad Serial FPDP PMC module was the first member of Tekmicro's new family of JazzFiber FPGA-based multiprotocol fiber-optic I/O modules. The JazzFiber PMC combines the advantages of the ANSI/VITA 17.1 Serial FPDP interconnect with highly integrated FPGA technology.

The use of a common FPGA architecture and software API allows applications to easily migrate between different JazzFiber solutions. The first JazzFiber protocol core supports ANSI/VITA 17.1 Serial FPDP. The JazzFiber PMC provides four fiber optic transceivers operating at up to 3.125 Gbits/s each, which can be configured as four independent interfaces or combined into a single 4x link. The JazzFiber PMC supports both PCI and PCI-X protocols at up to 133 MHz. A full gigabyte of onboard DDR SDRAM allows deep buffering of streaming data at the full 1 Gbyte/s data rate. Pricing starts at $7,995 for two-channel models and $9,995 for four-channel models in single-unit quantities.

TEK Microsystems
Chelmsford, MA.
(978) 244-9200.
[www.tekmicro.com].

RapidIO and Serial FPDP Links Supported on VME Blade

Intensive signal and data processing systems such as radar and imaging equipment place high demands on high-performance, low-latency throughput. Feeding such needs, Thales Computers offers its PowerNode5, the first dual 64-bit PowerPC970 VME blade server with backplane Serial RapidIO and Serial FPDP connectivity. The board is a rugged 6U VME PowerPC blade server featuring two 64-bit PPC970s running at 1.6 GHz. Its design is a clone of the IBM JS20 blade computer, providing the PowerNode5 with a very high level of performance and full binary compatibility with IBM JS20 blade servers, in a 6U form-factor fully adapted to any of today's embedded systems requirements.

Thales' Serial RapidIO switch fabric is an original implementation with a distributed Serial RapidIO architecture: each PowerNode5 is equipped with a 4-port switch allowing a flexible, full-mesh interconnect of up to four PowerNode5s and scalable up to a 16-PowerNode5 machine. The PowerNode5 features triple x4 Serial RapidIO links available on an enhanced performance P0 connector, compliant with legacy VME64x backplanes. The PowerNode5 is also available with a twin Serial RapidIO link plus a single Serial FPDP link option. The current version of the PowerNode5 blade computing node is currently shipping with an entry-level unit price of $9,670.

Thales Computers
Edison, NJ.
(732) 494-1011.
[www.thalescomputers.com].

XMC/PMC Features Quad Serial FPDP

FPDP offers many advantages as a point-to-point data link, and Serial FPDP does the same only faster. VMETRO expanded its range of high-performance PMC/XMC modules with the SFM Quad Serial FPDP module. The SFM supports up to four simultaneous serial FPDP (VITA 17.1-2003) channels. Until now, Serial FPDP cards have typically had just one channel. This new four-channel interface card provides a higher level of functional density without creating a bottleneck getting the data to and from the baseboard. The functional density and high performance is especially important for high-performance data recorders, high-channel density sensor arrays and high-end DSP systems. The simplicity and wide support for Serial FPDP make it ideal for a wide range of real-time embedded computer solutions.

In order to achieve optimal performance,

VMETRO implemented the SFM with separate DMA controllers for each channel. The SFM PMC module supports PCI-X data transfers at speeds up to 133 MHz. The SFM XMC module supports PCI Express via the XMC connectors and provides the full 2.5 Gbit/s data rate per channel. Using PCI-X and PCI Express this way enables more than one Serial FPDP transfer to happen simultaneously.

VMETRO
Houston, TX.
(281) 584-0728.
[www.vmetro.com].

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www.cotsjournalonline.com/getconnected

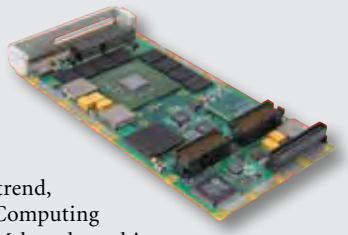
Upgraded AMC Serves Up Core2 Duo

The AdvancedMC (AMC) mezzanine form-factor is ramping up acceptance among military system designers. This trend will only increase as MicroTCA gains momentum as a backplane solution for AMC slot cards. For its part, Performance Technologies has announced an update to its AMC121 AMC single board computer that utilizes an Intel Core 2 Duo processor.

The upgraded module features a substantial increase in memory capacity—up to 4 Gbytes of 64-bit PC3200 DDR2 memory, as well as support for faster, user-replaceable, flash memory devices. The flash memory compatibility includes support for both standard MiniSD and high-capacity MiniSDHC modules and can be swapped out depending upon user requirements. This socketed option provides enhanced user flexibility to meet design requirements as opposed to permanently affixed flash memory devices that could limit module performance. The AMC's connector ports include two 1 Gbit to 2.5 Gbit Ethernet Channels, a pair of SATA links and eight PCI Express Lanes—x1, x4, or x8.

Performance Technologies, Rochester, NY. (585) 256-0200. [www.pt.com].

NVIDIA G73M Graphics Climb Aboard XMC



Graphics processing silicon developed for the gaming realm are used extensively in military graphics implementations. Exemplifying that trend, Curtiss-Wright Controls Embedded Computing has announced its first NVIDIA G73M-based graphics display control card, the XMC-710 XMC mezzanine module. This new COTS graphics card is the company's first designed to the new advanced XMC (VITA 42.3) open standard architecture, and is designed for use in VME, VPX and CompactPCI systems.

The XMC-710 graphics accelerator provides dual output and video capture capability. The card is powered by the NVIDIA G73M supported with a 128-bit local frame buffer interface with up to 512 Mbyte DDR2 frame buffer. To support customers with unique requirements, the XMC-710 was designed to adapt to and interoperate easily with different systems. An example of this built-in flexibility is the card's I/O mapping architecture, which simplifies adaptation to a specific host card's unique pinout configuration to ensure optimal I/O routing and video signal integrity. This flexibility enables system integrators to cost-effectively deploy the XMC-710 on third-party basecards. Pricing for the XMC-710 starts at $4,580. Evaluation units are available now, with production unit availability scheduled for Q2 2008. Both air-cooled and conduction-cooled versions, according to CWCEC ruggedization guidelines, are available.

Curtiss-Wright Controls Embedded Computing, Leesburg, VA. (703) 779-7800. [www.cwcembedded.com].

1500W Supply Designed for Harsh Environments

For harsh environment military applications, ordinary IT-class power supplies don't make muster. Serving such needs, Lambda has extended its 500-watt LZSa series of industrial power supplies to include 1000 and 1500-watt supplies with a unique feature set and safety-agency approvals not commonly found in standard off-the-shelf supplies. These new LZSa1000 and LZSa1500 series boast a wide operating temperature range, compliance with MIL-STD-810E standards for shock and vibration, and the ability to operate in explosive gas atmospheres.

These rugged power supplies are available with a nominal output of 12V (LZSa1000) or 24V (LZSa1000/1500). With integral fan-cooling, they provide full-rated output power from -40° to +60°C, derating linearly to 60 percent load at 71°C ambient. The LZSa series accepts a wide input range from 85 to 265 VAC, 47 to 440 Hz and has active power factor and harmonic correction. It also complies with SEMI-F47 standards for input droop down to 100 VAC at full load. Output ripple and noise is a low 75 mV peak-to-peak, and the unit is designed to provide 20-millisecond hold-up and ride-through to avoid nuisance tripping during transient electrical interruptions. The LZSa1000 and LZSa1500 are available now, priced at $825 and $1,250 each in 100-unit quantities.

Lambda Americas, San Diego, CA. (619) 575-4400. [www.lambdapower.com].

PC/104 SBC Suits Long Life Designs

Obsolescence is a constant disruptive force in the military market. Parts going end-of-life (EOL) are a fact of life. To address such needs, Acrosser Technology has introduced its AR-B8020, a low-power PC/104-Plus single board computer based on an RBC CPU. Many of the original low-end x86 CPU processors are currently being phased out. Although these products had a long life cycle, these CPUs are now End of Life (EOL). Due to recent EOL announcements on CPUs, Acrosser has developed the AR-B8020 to meet the demands of those still in need of these low-power devices. The RDC is a reliable, long-life CPU that not only meets customers' performance requirements, but also their low-cost targets. For these reasons, Acrosser choose the RDC 8610 to be the core of the AR-B8020.

The CPU is the 32-bit 8610 from RDC running at 133 MHz and the AR-B8020 is designed on the PC/104-Plus form-factor with onboard PC/104 and PCI-104 connectors for expansion boards. The board is Software compatible with DOS, Linux and Windows CE. I/O support includes 2 USB 2.0 ports, one 10/100 Ethernet port, three COM ports (one RS-232, two RS-232/485), one FDD, 1 x 44pin IDE and one 8-bit GPIO.

Acrosser Technology, Cypress, CA. (714) 903 1760. [www.acrosser.com].

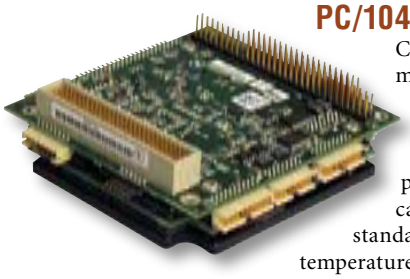
PCIe Card Sports 4-Channel 50 MS/s Digitizer/Scope

PCI Express was by no means the first switch fabric to enter the game, but it looks destined to be the most widely used, and the military market hopes to ride the wave. Supporting that trend, Strategic Test has introduced two 8-bit digitizer/oscilloscope PCI Express cards that support two and four 50 Msamples/s channels. The UF2e-2020 has two 50 Msamples/s channels, while the UF2e-2021 has four. Each channel has its own 8-bit ADC for simultaneous sampling, seven programmable input voltage ranges from ±50 mV to ± 5V, offset adjustment to 400 percent and both 50 ohm and 1 Mohm input impedances. Unique features of the UF2e-2020 and UF2e-2021 include the option for dual-timebase sampling, synchronous digital inputs, asynchronous digital I/O and the ability to synchronize up to 542 channels.

With up to 4 Gsamples of onboard memory, the cards are able to record signals for 40 seconds on two channels and 20 seconds on four channels. Alternatively, captured data can be streamed continuously to PC RAM or hard disk(s) at up to 120 Msamples/s over the PCIe bus. Prices start at $3,190 with volume/OEM discounts available.

Strategic Test, Woburn, MA. (617) 621-0080. [www.strategic-test.com].

PC/104-Plus SBCs Suit Up for Rugged Duties



Compute density has become the watchword in numerous military applications such as UAVs, vetronics and avionics systems. Feeding such needs, Parvus has unveiled its CPU-1472 and CPU-1474, two PC/104-Plus form-factor SBCs featuring the low-power Intel Celeron M 1 GHz processor and Intel i855GME chipset. The CPU-1472/74 cards operate without any active cooling (fanless) over standard (0° to +60°C) and extended (-40° to +85°C) operating temperature ranges. Like other Parvus/Eurotech CPU modules, system DRAM is soldered on board to enhance shock/vibration resistance, and each card is individually thermally qualified to ensure high reliability. A structural heat spreader plate is integrated on top of each CPU module to dissipate heat from critical components.

The CPU-1474 features dual Local Area Network (LAN) controllers (Gigabit and Fast Ethernet) and four USB 2.0 ports, along with standard PC peripherals and I/O interfaces, including dual serial ports, TFT/LVDS interfaces, AC97 audio interface, keyboard and mouse ports, and IDE controller. The CPU-1472 is similar but provides a total of eight USB 2.0 ports and a single 10/100 Ethernet controller.

Parvus, Salt Lake City, UT. (801) 483-1533. [www.parvus.com].

RF Test Tools Target Wireless Nets

Wireless networking is starting to pervade many kinds of military applications. To help test, troubleshoot, analyze and optimize such networks, Kaltman Creations offers a 2.4 GHz spectrum analyzer software package and a 2.4 GHz, 11-channel signal generator. Called the AirSleuth Pro and AirHorn (respectively), these products from Kaltman Creations are intended to address the RF side of the Wi-Fi and WLAN equation.

The AirSleuth Pro allows the user to view Wi-Fi channels 1 through 11 individually or simultaneously with Peak, Average and Raw trace modes. Working independently or in conjunction with AirSleuth Pro is a new product called AirHorn, a stable and accurate 2.4 GHz ISM band signal generator that can be selectively set to generate RF signals for any number of the 11 Wi-Fi channels.

The AirSleuth Pro is sold as a software-based application, which includes an antenna, user's guide and a frequently asked questions document. USB or PCMCIA versions are available for the same retail price of $395. AirHorn is also sold as a software-based application at a retail price of $135. The two are also bundled together for a combined price of $499.

Kaltman Creations,
Suwanee, GA. 678-714-200.
[www.kaltmancreationsllc.com].

XMC Blends Four Channels of 24-bit A-D Conversion

A mix of fast, precise analog-to-digital conversion is key in applications where vibration, acoustic and high dynamic range measurements are required. With just that in mind, an XMC I/O module from Innovative Integration features four simultaneously sampling, sigma delta A/D channels. The X3-SDF device has programmable output rates up to 24 bits at 2.5 Msamples/s and 16 bits at 20 Msamples/s using the programmable filter in the ADC. The X3-SDF module was developed in response to requests for DC-accurate measurements with very-wide dynamic range at sample rates up to 5 MHz.

A precision, low-jitter time base or external clock is used for sample rate generation. Sample rates up to 20 Msamples/s, with less than 10 kHz programmable resolution, are supported as well as external clocking. Trigger methods include counted frames, software and external triggering. Data acquisition control, signal processing, buffering and system interface functions are implemented in a Xilinx Spartan-3 1-million-gate FPGA. Two 1Mx16 memory devices are used for data buffering and FPGA computing memory. Quantity one pricing is $2,125.

Innovative Integration, Simi Valley, CA. (805) 578-4260. [www.innovative-dsp.com].

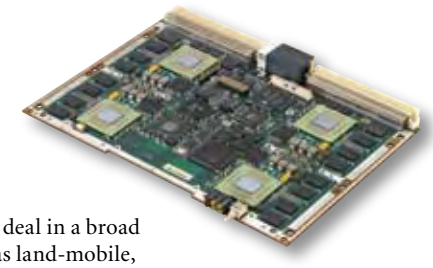
JTAG Platform Provides IEEE 1149.x for LXI

Following in the well-worn footsteps of VXI and PXI, the LXI interface has now become entrenched as a LAN-based interconnect for instrumentation applications. Its use of Ethernet fits well into the military's growing affection for networked-based designs. With that in mind, Goepel Electronic has rolled out a new series of specific JTAG/Boundary Scan controllers with LXI Interface, called the SFX/LXI1149-(x), which supports JTAG/boundary scan solutions compliant with IEEE Std.1149.x.

Available in three performance classes A, B and C, the models differ in the maximum TCK frequency (20, 50 and 80 MHz, respectively) and in the degree of implementation of the enhanced Space chip set for high-performance scan operations. In contrast to conventional solutions, the integrated Fastscale technology allows an upgrade of the controller's performance class "on the fly," without intricate mounting of additional hardware. SFX/LXI1149-(x) is a LXI Class-C device and provides a Triple Speed Ethernet-Interface (10/100/1000 Mbit/s). It is compliant with LXI hardware specification 1.1 and can be remote configured via the integrated Web browser.

Goepel Electronic, Jena, Germany. +49-3641-6896-739. [www.goepel.com].

Dual-Core PowerPC VXS Card Aims at DSP Apps



Compute density is a big deal in a broad range of applications such as land-mobile, airborne fixed and rotary wing, and naval surface and underwater platforms that require a high-performance multiprocessor. Feeding such needs, the DSP220 from GE Fanuc Intelligent Platforms provides four single- or dual-core Freescale PowerPC 8641 system-on-chip nodes and a VITA 42.2-compliant XMC slot. This 6U VXS (VITA 41.2) multicomputer is designed for demanding signal and data processing applications and is available in six ruggedization levels including air-, spray- and conduction-cooled for extended temperature operation as well as resistance to shock and vibration.

The DSP220 derives its performance from a number of key features. Each PowerPC e600 core is clocked at 1 GHz, and each 8641 node supports two banks of DDR2 SDRAM with 256 Mbytes per bank, 2 Gbytes total per card, as standard. Up to 8 Gbytes SDRAM per board is optionally available. The multi-fabric data plane interfaces include Tundra Serial RapidIO to all 8641 nodes, XMC site and the system backplane along with two Gbit Ethernet ports to all nodes and off board for optimum system throughput. System management and additional data movement options are supported over the VME64 2eSST interface.

GE Fanuc Intelligent Platforms, Charlottesville, VA.
(800) 368-2738. [www.gefanuc.com].

System Embeds Stacked PCI-104 Modules

Many military applications depend on reliable data acquisition, along with resistance to extreme temperature fluctuations, shock and vibration. To meet this demand for a highly modular, compact and rugged solution, Advantech has added a new compact embedded computer to its ARK-4000 product series. The ARK-4180 is a PCI-104-based solution with high vibration/shock resistance and wide temperature capability. The ARK-4180 with Intel Celeron M 1.0 GHz processor can operate in temperatures ranging from -40° to 75°C, providing high processing performance in a compact, rugged enclosure.

The ARK-4180 is developed from PCI-104 stackable modules that are designed and qualified for demanding applications. The PCI-104 form factor allows modules to stack vertically to provide a naturally rugged architecture. Each system is housed in a specially cast and milled solid aluminum block with thermal fins that help dissipate heat. Another feature is the specially designed fanless thermal solution with embedded heat pipes, which allow wide temperature operation without active cooling. The ARK-4180 supports six USB 2.0 and two RS-232 connectors, 10/100Base-T Ethernet LAN and VGA for versatile connectivity. It supports one PCI-104 connector for expansion, and by adding another enclosure layer, up to two more PCI-104 modules can be stacked.

Advantech, Irvine, CA. (949) 789-7178. [www.advantech.com].

Box-Level System Supports PMC, PC/104 Expansion

The stand-alone rugged box trend has opened up a whole set of product choices for military system designers. To date many such systems have been on the expensive side. Offering a low-cost alternative, Adlink Technology offers its compact PC-based controller system. The GEME-42000 from Adlink Technology is equipped with an Intel Ultra Low Voltage Celeron M processor (1.0 GHz) and up to 1 Gbyte of DDR333 RAM, and can be controlled from remote locations and run continuously in mission-critical applications.

The GEME-42000 meets the needs of embedded controllers; it is compact, has front side access, is highly reliable and offers an expandable architecture with optional motion, I/O and communication modules in PMC or PC/104 form-factors. Power supply options include standard AC power for stationary applications and DC power for mobile applications such as in vehicles. Supported operating systems include Windows XP Embedded, WinCE .Net and Linux. The GEME-42000 is priced at $925 with discounts in volume.

Adlink Technology, Irvine, CA. (970) 377-0385. [www.adlinktech.com].

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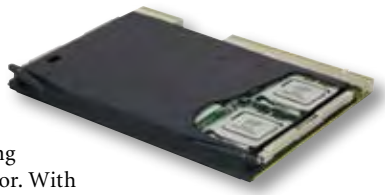
Conduction-Cooled cPCI SBC Sports 16 Gbytes of DRAM



Technology upgrades are a staple of military system designs. Programs want the latest and greatest processing and memory, but in a tried and true standard form-factor. With just that in mind, General Micro Systems has developed a fifth-generation dual-processor, rugged SBC. The conduction-cooled CompactPCI CC279 "PREMONITION" offers exceptional speed and memory—delivering four times the performance of previous in-a-single-slot, convection-cooled SBCs. The CC279, which supports Intel's ultra-fast Virtualization Technology, is powered by two Quad Core Xeon processors, operating at up to 1.6 GHz, or two Dual Core Xeon processors, operating at up to 2.33 GHz. The result, with up to eight independent processors on a single-slot board, is unprecedented performance at only 100W in a conduction-cooled design.

Each of the two 8 Gbyte, 144-bit ECC memory banks functions independently of the other at 10.6 Gbytes/s, providing an effective memory transfer rate of 21.6 Gbytes/s. Standard I/O functions include Quad GigE Ethernet ports with a TCP/IP Offloading engine, six USB-2.0, one Com port with RS-232/422, 20 GPI/O lines, six SATA-2 ports with RAID support and one PATA port. The CC279 is hot swappable with auto config System Master/Peripheral Master, supporting PICMG 2.16 and PICMG 2.9. Pricing for the PREMONITION (single units) starts at $8,300.

General Micro Systems, Rancho Cucamonga, CA. (909) 980-4863. [www.gms4sbc.com].

Microwave Signal Generator Has Fast Switching

Many military development projects require a wide range of broadband measurements. Among these are EW, radar, military communications and wireless applications. With all that in mind, Agilent Technologies has announced the availability of a compact microwave analog signal generator that delivers a low cost of ownership and is an extension to the popular Agilent MXG signal generator platform, providing frequency coverage to 20, 32 or 40 GHz.

The Agilent N5183A MXG is an economy-class, continuous wave (CW) signal generator specifically designed to maximize uptime and reduce cost of ownership. Its less than or equal to 900 microsecond switching speed enables a dramatic increase in throughput. Another key feature of the Agilent N5183A MXG is its outstanding performance. With +18 dBm to 20 GHz output power, it is able to overcome losses and drive high-power devices. Additionally, it features a level accuracy, with optional step attenuator, of ±0.6 to 0.8 dB. Other options to the Agilent N5183A MXG include analog modulation and pulse modulation—all housed in a compact 2U (3-inch high) package that better uses rack space. Agilent's new N5183A MXG microwave analog signal generator is now available. Pricing ranges from $18,000 to $30,000.

Agilent Technologies, Santa Clara, CA 95052. (800) 829-4444. [www.agilent.com].

Multiview Display Does 1920 x 1080p HD

Complex real-time video and graphics data are rolling in with the military's vision of Network-Centric operations. Enabling that drive, Zandar Technologies offers a set of multimedia display solutions, including its FusionPro+ multiviewer. Zandar Technologies was recently acquired by Harris, and together they now offer the widest range of multiviewers available in the industry. The FusionPro+ multiviewer is part of the new family of multiviewers offered by Harris. It is a multi-image display solution for mission-critical security monitoring and surveillance. The 1RU unit displays up to eight channels, and the 3RU unit displays up to 26 channels.

The FusionPro+ can take any mix of analog, SDI, HD-SDI and computer inputs, and display them on a single screen with output up to HD (1920x1080p). An additional feature is the ZdH Dual output option. In addition to the FusionPro+, the new range of multiviewers by Harris Corporation includes the recently introduced Zandar Predator II multiviewer. Specifically designed for control and monitoring, the 2RU Predator II multiviewer can handle up to 32 HD, SD and analog inputs and is perfectly suited for various applications, including command centers, master control, AV applications, security monitoring and surveillance.

Harris, Melbourne, FL.
(321) 727-9100. [www.harris.com].

Center Probe Test Socket Supports Up to 18 GHz.

The electronics industry has moved solidly into the "GigaHertz" era, with all the complexities that entails, and the military is the front row of customers demanding such performance. Aimed at easing the pain of fast signals, Aries Electronics has announced its new high-frequency center probe test socket for devices up to 13 mm squared. Available in four versions with ratings of 1-3 GHz, 3-5 GHz, 5-9 GHz and 10-18 GHz, the new socket is ideal for manual, high-speed testing of devices such as CSP, mBGA, DSP, LGA, SRAM, DRAM and flash, with pitches as low as 0.40 mm.

The socket's solderless, pressure-mount, compression spring probes allow the socket to be easily mounted to and removed from the test board. The socket's contact forces are 16g per contact on a 0.50 mm pitch, 25g per contact on a 0.50-0.75 mm pitch and 25g per contact on 0.80 mm or larger pitch. Operating temperature is -55° to 150°C and estimated contact life is more than 500,000 cycles. Pricing for a center probe test socket with up to 50 positions starts at $330 in single piece quantities.

Aries Electronics, Bristol, PA. (215) 781-9956. [www.arieselec.com]

System Links Multi-Slot PCI Express to PCI

The speed and bandwidth of PCI Express has transformed military test and measurement so that now complex tasks can be done in a single PC-based system. Adlink Technology has introduced a new series of multi-slot PCI Express-to-PCI extension systems: the PCES-8581-4S, offering expandability to four PCI slots, and the PCES-8581-13S, offering expandability to 13 PCI slots. The PCES-8581 series extends 5V and 3.3V PCI slots to a PCI Express-based computer via a cable connection up to 23 feet (7 meters) in length.

The PCES-8581 expands the I/O capability of measurement and automation systems beyond the limited number of onboard PCI slots common in host systems. They also provide a ruggedized extension system that can withstand high temperatures and harsh vibrations so that host systems with a PCI Express x1 interface can both be located at a safe distance from such environment and directly control remote PCI devices. The PCES-8581-13S and PCES-8581-4S both implement PCI Express-based control of PCI modules and consist of a PCI Express extension card installed in the host computer, a shielded cable and the extension system. Both the PCES-8581-13S and PCES-8581-4S are currently available and are competitively priced at $1,499 and $1,199, respectively, with discounts in volume.

Adlink Technology, Irvine, CA. (970) 377-0385. [www.adlinktech.com].

Digital Instrumentation Set Leverages USB

Where once only large racks of boards were needed, now complex military test platforms can be implemented with USB-based modules hosted by a PC. Fueling just that trend, National Instruments has rolled out its NI USB-5132/5133 digitizers and the NI USB-4065 6½-digit digital multimeter (DMM). These small, lightweight instruments feature bus-powered and plug-and-play operation, which makes them ideal for portable, benchtop and OEM applications. They also are shipped with NI LabVIEW SignalExpress LE interactive measurement workbench software for quickly acquiring, analyzing and presenting data with no programming required.

The USB-5132/5133 50 Msample/s and 100 Msample/s digitizers offer two simultaneously sampled channels with 8-bit resolution. These USB digitizers feature 10 input ranges from 40 mV to 40V and programmable DC offset, and come standard with 4 Mbytes/channel of onboard memory for measurements requiring extended data captures. The USB-4065 DMM offers 6½ digits of resolution at up to 10 readings per second and up to 3,000 readings per second at lower resolutions. With ±300V of isolation, current measurements up to 3A and 2- or 4-wire resistance measurements, the USB-4065 offers a complete multimeter solution for portable 6½-digit measurement needs. Pricing for these products ranges from $899 to $1,299.

National Instruments, Austin, TX. (512) 683-0100. [www.ni.com].

Rad-Hard FPGAs Boast Four-Million Gates

An embedded system designed to travel through space needs electronics that are uniquely suited for the environment. Now even high-density FPGAs are entering that arena. An example is the RTAX4000S device from Actel. This four-million-gate radiation-tolerant RTAX-S FPGA has completed the stringent MIL-STD-883 Class B qualification. The RTAX4000S device has completed 1,000 hours of high-temperature operating life (HTOL) testing and nearly 80,000 total hours of life testing data to date. This device-specific testing data is in addition to the more than 2,000,000 device hours of testing and rapidly accumulating flight heritage achieved by the remainder of the RTAX-S family. The qualification of the device, combined with its usable error-corrected onboard memory and large number of user I/O, make it ideal for high-bandwidth processing applications in spacecraft payloads. Rigorous testing and qualification of the RTAX4000S toward QML Class Q and QML Class V certification continues.

Hardened by design against radiation single-event upsets (SEUs), the nonvolatile RTAX4000S requires no radiation mitigation techniques. Competing high-density FPGA solutions require user-instantiated triple module redundancy (TMR), which can consume more than two-thirds of the device's available logic. The RTAX4000S offers the inherent flexibility of the programmable fabric, delivering cost and time-to-market advantages over radiation-hardened (RH)-ASICs.

Actel, Mountain View, CA. (650) 318-4200. [www.actel.com].

VME/VXS Board Supports Multiple Gbit Links

Military systems requiring wideband, data-acquisition and recording, real-time digital signal-processing all have something in common. They need a hefty blend of real-time signal processor and fast interconnect to get the data where it needs to go. Pentek achieves all that with its Model 4207, a VME/VXS card. In addition, Pentek's unique fabric-transparent crossbar switch bridges a wealth of Gbit serial resources, including the PowerPC and FPGA, two XMCs, dual VXS ports, dual Fibre Channel ports and two optical serial transceivers. Native protocols support PCI Express, Serial RapidIO, Fibre Channel and Aurora, all accommodated by the crossbar switch. Up to 4 Gbytes of fast DDR2 SDRAM simplifies data buffering and boosts real-time signal processing.

The fabric-transparent crossbar switch of the Model 4207 offers extraordinary high-speed connectivity. Since the processor configures all routing paths, the switch simply passes the gigabit serial traffic from one port to another, totally independent of any particular protocol. Multiple data streams can be sent through the switch simultaneously, even if they have different protocols. Pentek's Model 4207 is immediately available. Because all high-speed interfaces on the board connect through the switch, paths can be configured to meet specific requirements. Pricing starts at $14,725.

Pentek Upper Saddle River, NJ. (201) 818-5900. [www.pentek.com].

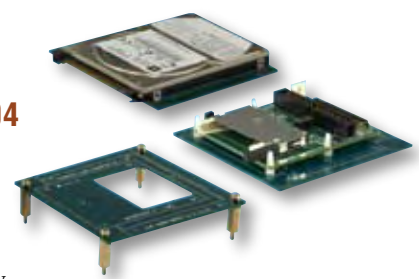
VPX Carrier Boards Support XMC, PMC

The carrier board concept has served the military industry well. The legacy of VME carriers and their mezzanines has been a tried and true approach for mixing and matching system functionality. Now that concept has been carried forward in the new generation of form-factors: VPX and XMC. With that in mind, VMETRO offers two new products, the MM-1200, an intelligent 6U XMC/PMC carrier, and VCX301, a 3U XMC carrier. The MM-1200 and VCX301 are suited for use in deployed signal processing systems such as electronic warfare (EW) and Intelligence, Surveillance and Reconnaissance (ISR) applications.

Based on the 6U VPX form-factor, the MM-1200 is an Intelligent XMC/PMC Carrier. This board enables onboard devices including the XMC/PMC sites, large SDRAM memories and the onboard CoSine System-on-Chip to directly interface with a Serial RapidIO-based fabric. The CoSine Systems-on-Chip are fully functional computers with dual embedded PowerPC 405GPs for a total of 4 embedded PowerPC processors. The MM-1200 design was based on VMETRO's existing VPX board, the MM-1600, which has two additional large Xilinx Virtex-4 FPGAs. Both products are available as air- or conduction-cooled rugged versions.

VMETRO Houston, TX. (281) 584-0728. [www.vmetro.com].

Adapter Kits Boost Functionality of PC/104



The unique stacked configuration of PC/104 enables military system designers to craft a compact, rugged embedded computing solution. Bringing that to a new level, Sealevel Systems has introduced adapter kits that greatly improve the functionality of PC/104 stacks by making it easier to include CompactFlash memory, hard drives and other common devices. The kits are mechanical adapters that mount to the PC/104 stack but do not interface to the stack; the interface is made using the IDE or USB connector on the device being added. The mounting holes on the adapters are arranged with slots at the corners so the board can be mounted in line with the PC/104 stack or rotated 180 degrees along the long axis.

The PC/104 adapter kit product line is available as a CompactFlash memory adapter, 2.5-inch hard drive adapter and a multipurpose adapter. All kits include standard 0.60-inch aluminum standoffs for mounting to the PC/104 stack. The PC/104 multipurpose adapter is a versatile device that allows users to add Sealevel OEM products including SeaDAC Lite modules and embedded 4-port USB hub. The PC/104 CompactFlash adapter (CF104) is $90. The PC/104 hard drive adapter (Item# HD104) is $30. The PC/104 multipurpose adapter (PH104) is $15.

Sealevel Systems, South Carolina, SC.
(864) 843-4343. [www.sealevel.com].

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PC/104-Plus SBC Withstands Extended Temps

PC/104's popularity continues to ramp for military applications where space constraints and power concerns are priority. Fastwel's latest PC/104-Plus single board computer offering is the CPC304. Based on the AMD Geode LX800 CPU and AMD CS5536 I/O companion chipset, the board provides full support for PC/104 and PC/104-Plus expansion modules. The board is designed for use in mission-critical, onboard systems requiring low power consumption and wide operating temperature range from -40° to +85°C. All key components including CPU, chipset, memory and peripheral controllers are soldered onboard providing excellent vibration stability and increased efficiency.

A protective conformal coating is available to enhance the survivability of the board in exposed or other harsh environments. System developers can take advantage of simultaneous operation of a standard VGA interface with resolution up to 1920x1440, or 24-bit LVDS interface for connection of TFT or DSTN LCD panels. For data exchange CPC304 offers two independent Fast Ethernet ports, four COM ports, two USB 2.0 ports and eight programmable discrete input/output lines. The CPC304 will begin shipping in volume in March with prices starting at $658.

Fastwel, Brooklyn, NY.
(718) 554-3686. [www.fastwel.com].

Module Offers Dual 14-Bit ADC/DAC I/O

Applications like software defined radio (SDR) are hungry for compact, modular data conversion. Feeding that need, iVeia has introduced the GigaFlex 220, a high-speed analog-to-digital and digital-to-analog I/O module designed for the iVeia Titan family of processing modules. The GigaFlex 220 adds two 14-bit 150 MSPS ADCs and two 14-bit 1 GSPS DACs to a Titan processing module creating a small form-factor platform ideal for intermediate frequency (IF) processing in SDR applications.

Only 2.125 x 3.525 x 4.25 inches in size, the module has advanced clock generation circuitry that allows the software to independently set the sample rates of the dual ADC and dual DAC to almost any frequency. The GigaFlex 220 has a clock generator that can phase-lock to the onboard 10 MHz TCXO reference or an optional external reference. Through the Digital I/O Connector, the GigaFlex 220 provides one to two RS-232 UARTs and five bi-directional general-purpose I/Os (GPIOs). The GPIOs may be used for time (1 PPS, IRIG-B and so on), synchronization, or custom user-programmable I/O. The product operates over temperature ranges of -40° to 85°C.

iVeia, Annapolis, MD. (410) 858-4560. [www.iveia.com].

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Coming Next Month

- COTS Journal *10th Anniversary Military Market Perspectives Special*. Yes, it's true. *COTS Journal* turns 10 years old this month. To celebrate the occasion this special section will enlist some key contributors to offer their insights on how the military market has evolved over the past decade and on what the next decade will hold.
- *VPX, VXS and VME—the Staple for Many Military Systems*. VME has earned an enduring role as the most popular embedded computer form-factor for defense applications. Next-generation, fabric-based flavors of VME are coming together in the form of specs such as VXS (VITA 41) and VPX (VITA 46). This section updates readers on the progress of those implementations and displays a sampling of the current crop of VME, VXS and VPX single board computer (SBC) products.
- *Annual End-of-Life Directory*. Its unique coverage of key military technology issues in a way that you can't find elsewhere: that's what *COTS Journal* is known for. Exemplifying that unique character is our *Annual End-of-Life Directory*. Now in its 9th year, the EOL Directory lists both key DoD organizations and commercial firms involved in solving the problems of component obsolescence. The section also examines how those obsolescence issues are complicated by Europe's RoHS initiative.
- *Rugged Ethernet Switch Boards*. Ethernet is becoming entrenched as a favorite interconnect fabric in compute-intensive applications like sonar, radar or any application that networks sensor arrays together. This section updates readers on the product and technology trends driving board-level Ethernet switch products, and will include a product album of representative Ethernet switch board products in form-factors such as VME, cPCI, MicroTCA and more.


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Editorial

Jeff Child, Editor-in-Chief

Defense Industry's Quality Quest

I don't know what it is about *COTS Journal* readers, but you are indeed an alert and watchful bunch—even on the most minute details. Two times in this magazine's history we got the Volume and Issue number wrong on our table of contents page, and readers e-mailed me on both of those occasions to inform me of the error. That kind of thing pleases me for two reasons. First, it keeps us on our toes, and second, it's evidence that you're reading us intently and I'm gratified by that.

Quality is important to us, and I have no doubt that quality design and manufacturing is something that people at every tier of the defense industry food chain take seriously too. All that said, it should come as no shock to anyone that the defense industry has a less than stellar track record when it comes to quality. If a quality product is defined as one that's delivered on time, performs as expected, and can be depended on to perform when needed, at an affordable cost, one can't ignore that many programs fall short in these areas. It's rare that a consumer electronics manufacturer is unable to get its product on the store shelves in time for the holidays. But it's all too common that a prime contractor fails to deliver a major weapons system on time and on budget.

Mistakes are inevitable in any endeavor, but avoiding them always comes down to "process." With her skilled eye for detail, our talented copy editor Rochelle thoroughly poured over the piece you're reading right now and fixed my mistakes. Then I looked at it again, and then she looked at it again when the page was laid out, and ultimately I gave this and every page in the magazine a final look. Forgive me that clumsy example—the complexity of putting out a magazine is infinitesimal compared to developing and building, for example, an advanced jetfighter. My point is simply that quality and process are intertwined and vital to satisfying the customer. If we got into the habit of spelling "infinitesimal" wrong, I have no doubt that our readers and customers would notice.

Yes, in many ways my earlier comparison of the consumer electronics vendor and the defense contractor is apples and oranges. But the contrasts between the two are very telling. When it comes to achieving quality, the defense industry has some factors stacked against it—just by the nature of what it builds and its culture. The DoD acquisition environment really lacks any incentives for prime contractors to use best practices to efficiently build high-quality weapon systems.

A GAO report called "Best Practices: Increased Focus on Requirements and Oversight Needed to Improve DOD's Acquisition Environment and Weapon System Quality," released earlier this month, delved deep into these challenges of quality in the defense industry. The report examined eleven DoD weapon systems with known quality problems and took an interesting look at the commercial practices that can be used to improve DoD weapon systems.

The report points out how, during the systems development of a military program, the DoD generally pays the costs incurred for the contractor's best efforts and accepts most of the financial risks associated with development. It does that because of the technical uncertainties. It's also typical that the DoD and its contractors enter into development contracts before requirements have been analyzed with disciplined systems engineering practices. In those cases, costs and schedule can go awry during development and there's no risk borne by the prime contractor. In contrast, commercial companies—like our consumer electronics example earlier—operate in an environment that requires their own investment of significant funds to develop new products before they are able to sell them and recoup that investment. That creates incentives for continuous improvement in systems engineering, manufacturing and supplier quality activities.

Another issue affecting quality is the tendency to jump quickly into the development phase of a program. You see that particularly in the case of advanced and complex transformal programs like the Army's FCS program, the Navy's DD(X) program, the Air Force's Transformational Satellite (TSAT) program and the Joint Tactical Radio System (JTRS) program. Concerns continue to mount as to whether those future-looking programs jumped too quickly into a pure "systems engineering" phase, while leaving out ample room for experimentation and discovery. Because of that, two things end up happening: Program requirements are set without adequate systems engineering knowledge. And without requirements that have been thoroughly analyzed for feasibility, development costs are impossible to estimate and as a result are destined to grow out of control.

While attempts have been made to reform the practices and procurement efficiency in the defense industry, it's a beast that's notoriously slow to change. It's encouraging at least that the industry's quest for improving quality is being discussed and scrutinized. Now, if you will excuse me, I need to go double-check that we've got the Volume and Issue number right in the table of contents this month.

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